QUESTION 1.

4 **(a)** Three descriptions and two types of processor are shown below.

Draw a line to connect each description to the appropriate type of processor.

Description	Type of processor
Makes extensive use of general purpose registers	RISC
Many addressing modes are available	CISC
Has a simplified set of instructions	

[3]

(b) In a RISC processor three instructions (A followed by B, followed by C) are processed using pipelining.

The following table shows the five stages that occur when instructions are fetched and executed.

(i) The 'A' in the table indicates that instruction A has been fetched in time interval 1.

Complete the table to show the time interval in which each stage of each instruction (A, B, C) is carried out.

Stage	Time interval								
	1	2	3	4	5	6	7	8	9
Fetch instruction	A								
Decode instruction									
Execute instruction									
Access operand in memory									
Write result to register									

[3]

(ii) The completed table shows how pipelining allows instructions to be carried out more rapidly. Each time interval represents one clock cycle.

Calculate how many clock cycles are saved by the use of pipelining in the above example.

Show your working.

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[3]

QUESTION 2.

2 **(a)** The following diagram shows four descriptions and two types of processor.

Draw lines to connect each description to the appropriate type of processor.

Description	Type of processor
It has a simplified set of instructions.	
Emphasis is on the hardware rather than the software.	CISC
It makes extensive use of general purpose registers.	RISC
Many instruction formats are available.	

[4]

(b) In a RISC processor, instructions are processed using pipelining.

(i) Explain what is meant by **pipelining**.

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.....[2]

(ii) The following table shows the five stages that occur when instructions are fetched and executed. The table also shows a number of time intervals.

Two instructions, D followed by E, are fetched and executed. The 'E' in the incomplete table shows that instruction E has been fetched in time interval 2.

Complete each row of the table.

	Time interval							
Stage	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Fetch instruction		E						
Read registers and decode instruction								
Execute instruction								
Access operand in memory								
Write result to register								

[3]

(c) The instruction set for a RISC processor that allows pipelining include
instruction.

Instruction		Explanation
Op code	**Operands**	
`ADD`	`<dest>, <op1>, <op2>`	Add the integers in registers `op1` and `op2`. Place the result in register `dest`.

A program contains the following three instructions.

```
ADD r3, r2, r1

ADD r5, r4, r3

ADD r10, r9, r8
```

(i) Explain why pipelining fails for the first two instructions.

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.....[2]

(ii) The instructions were produced by a compiler after translation of a high-level language program.

The compiler is not capable of code optimisation.

State how the code from the compiler could have been optimised to overcome the problem in **part (c)(i)**.

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.....[1]

QUESTION 3.

[1]

5 **(a)** Most desktop or laptop computers use CISC (Complex Instruction Set Computing) architecture. Most smartphones and tablets use RISC (Reduced Instruction Set Computing).

State **four** features that are different for the CISC and RISC architectures.

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2 .....

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[4]

(b) In a RISC processor, four instructions (**A**, **B**, **C**, **D**) are processed using pipel

The following table shows five stages that take place when instructions are fe executed. In time interval **1**, instruction **A** has been fetched.

(i) In the table, write the instruction labels (**A**, **B**, **C**, **D**) in the correct time interval for ea stage. Each operation only takes one time interval.

Stage	Time interval								
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Fetch instruction	**A**								
Decode instruction									
Execute instruction									
Access operand in memory									
Write result to register									

[3]

(ii) When completed, the table in **part (b)(i)** shows how pipelining allows instructions to be carried out more rapidly. Each time interval represents one clock cycle.

Calculate how many clock cycles are saved by using pipelining in the example in **part (b)(i)**.

Show your working.

Working .....

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Answer .....

[3]

(c) The table shows four statements about computer architecture.

Put a tick (✓) in each row to identify the computer architecture associated with each

Statement	Architecture		
	SIMD	**MIMD**	**SISD**
Each processor executes a different instruction			
There is only one processor			
Each processor executes the same instruction input using data available in the dedicated memory			
Each processor typically has its own partition within a shared memory			

QUESTION 4.

7 **(a)** RISC (Reduced Instruction Set Computing) and CISC (Complex Instruction
are two types of processor.

Tick (✓) **one** box in each row to show if the statement applies to RISC or CISC proce

Statement	RISC	CISC
Larger instruction set		
Variable length instructions		
Smaller number of instruction formats		
Pipelining is easier		
Microprogrammed control unit		
Multi-cycle instructions		

[3]

(b) In parallel processing, a computer can have multiple processors running in parallel.

(i) State the **four** basic computer architectures used in parallel processing.

1 .....

2 .....

3 .....

4 .....

[4]

(ii) Describe what is meant by a **massively parallel computer**.

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..... [3]