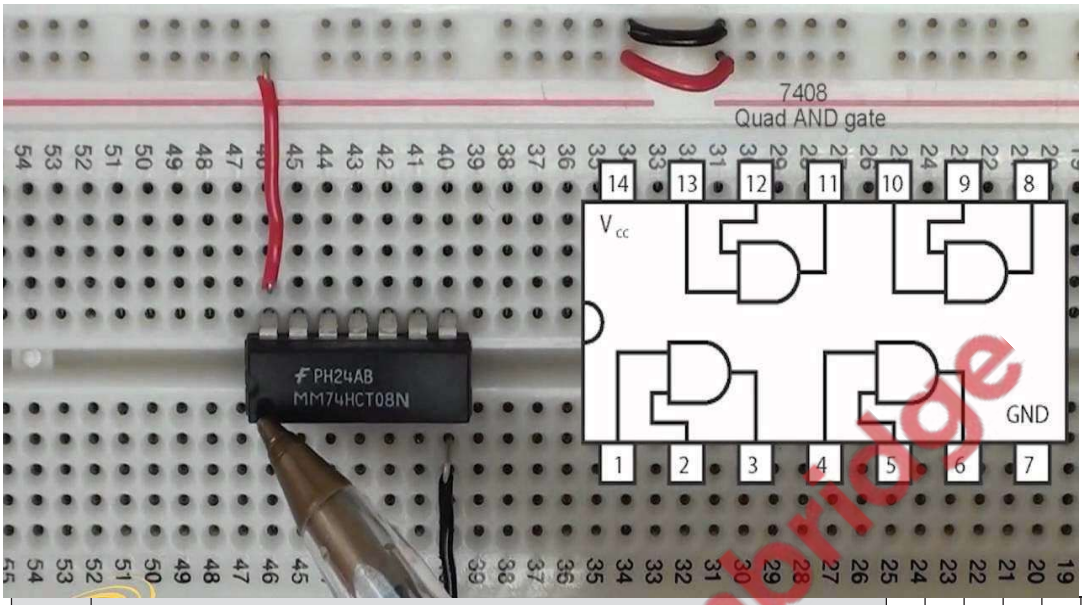
1.3.1 Binary Logic FOR IGCSE

Chapter 3

1.3.1 Binary Logic



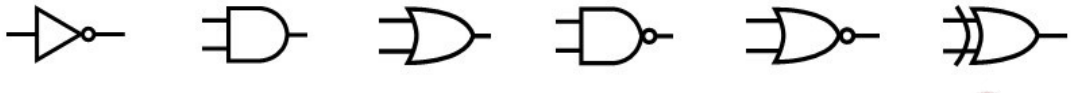
S No	Learning Outcome	To Read	Have Read	To Revise	Have	Prepared
	1.3.1: Logic gates					
22	use logic gates to create electronic circuits					
23	Understand and define the functions of NOT, AND, OR, NAND, NOR and XOR (EOR) gates, including the binary output produced from all the possible binary inputs (all gates, except the NOT gate, will have 2 inputs only)					
24	Draw truth tables and recognise a logic gate from its truth table					
25	Produce truth tables for given logic circuits,					
26	Produce a logic circuit to solve a given problem or to implement a given written logic statement					
27	Write down logic statement of given logic circuit					
28	Simplify the logic circuit					
29	Boolean algebra					
30	Solving past paper questions					

1.3.1 Logic Gates

Many electronic circuits have to make decisions. They look at two or more inputs and use these to determine the outputs from the circuit. The process of doing this uses electronic logic, which is based on digital switches called **Logical Gates.**

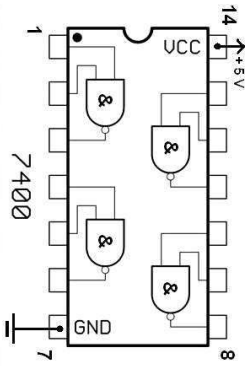
Logic gates are devices that can combine multiple inputs at independent logic levels and come up with an output accordingly. They are used by implementing Boolean algebra. Logic gates have two or more input and one output except NOT Gate which has one input and one output.

The most common Logical Gates are given below:



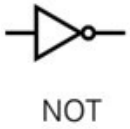
For example, The most obvious use is for simple control. Imagine designing a washing machine so that the water only turns on when the washing is loaded (logic-1), the door is closed (logic-1) but the clothes are not yet wet (logic-0). This can be done by ANDing the first two conditions, and inverting the third. Now, AND these together, and you get a high only when all three conditions are satisfied.

Two or more logic gates can be connected to produce a logic circuit with one or more outputs from two or more inputs.



1) NOT Gate (Inverter):

A **NOT gate** or an **inverter** is the simplest kind of logic gate. Its function is to give the opposite output to its input - if it gets a high (1), it gives a low (0), and vice versa. This is equivalent to saying that the output is *not* the input.



NOT

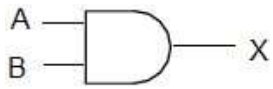
NOT Gate	
Input A	Output X
0	1
1	0

The output X) =1 if
INPUT A is **NOT 1** (i.e. **0** or **OFF**).

$$X = \overline{A}$$

2) AND Gate

An **AND gate** gives an output 1 only when both inputs are 1.
If one or more inputs are 0, then the output is also 0.



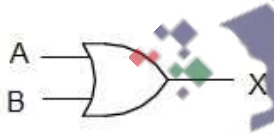
Input A	Input B	Output x
0	0	0
0	1	0
1	0	0
1	1	1

The output X=1 IF both inputs are 1.
The output (called X) is **true** (i.e. **1** or **ON**) only if the (**INPUT A AND INPUT B**) are both **true** (i.e. **1** or **ON**).
The x=1 if
INPUT A is 1 AND INPUT B is 1

$$X = A \,.\, B$$

3) OR Gate

An **OR gate** gives a high (1) output if any input is high (1). If all inputs are low (0), then the output is low (0).



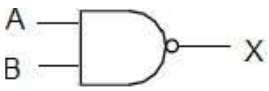
Input A	Input B	Output x
0	0	0
0	1	1
1	0	1
1	1	1

The output X=1 IF Any one Input is 1.
The output (called X) is **true** (i.e. **1** or **ON**) if the (**INPUT A OR INPUT B**) are **true** (i.e. **1** or **ON**).
The OUTPUT X=1 IF
Either INPUT A is 1
OR INPUT B is 1

$$X = A + B$$

4) NAND Gate

This NOT AND combination is shortened to just NAND. A **NAND gate** gives a 0 output only when both inputs are 1. If one or more inputs are 0, then the output is 1.



Input A	Input B	A AND B	OUTPUT X
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

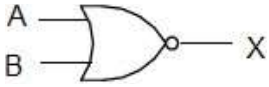
The output X=0 IF both inputs are 1.

The output (called X) is **true** (i.e. **1** or **ON**) if (**INPUT A AND INPUT B**) are **NOT** both **true** (i.e. **1** or **ON**) is 1

$$\boldsymbol{X = \overline{A \,.\, B}}$$

5) NOR Gate

This NOT OR combination is shortened to just NOR. A **NOR gate** gives a 0 output if any input is 1.



Input A	Input B	A OR B	OUTPUT X
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

The OUTPUT x=0 IF

either A is 1 OR INPUT B is 1

$$\boldsymbol{X = \overline{A + B}}$$

6) XOR Gate

The '**Exclusive-OR**' gate is a circuit which will give a 1 output if **either, but not both**, of its two inputs are 1. If both inputs are same then output will be 0 else output will be 1

Input A	Input B	Output x
0	0	0
0	1	1
1	0	1
1	1	0

The OUTPUT X=1 IF

Either A is 1 AND B is NOT 1

OR A is NOT 1 AND B is 1

Or it may be said that X=1 If A is 1 OR B is 1 **BUT NOT BOTH**

$$\boldsymbol{X = \left(A \,.\, \overline{B}\right) + \left(\overline{A} \,.\, B\right)}$$

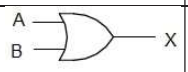
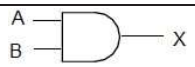
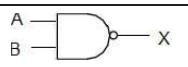
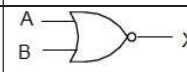
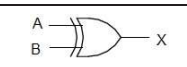
Truth tables

"A truth table is used to show the output of a logic gate or circuit for all possible combinations of input values."

Usually the binary values are used, 1 and 0, as shorthand for True and False.

The truth table for a two-input gate needs four rows (2^2=4) while for 3-input gate needs eight rows (2^3=8).

The truth table for a two-input gate needs four rows.

INPUT		OR	AND	NAND	NOR	XOR
A	B					
		$X = A + B$	$X = A.B$	$X = \overline{A.B}$	$X = \overline{A + B}$	$X = (A.\overline{B}) + (\overline{A}.B)$
0	0	0	0	1	1	0
0	1	1	0	1	0	1
1	0	1	0	1	0	1
1	1	1	1	0	0	0

Logic circuits

Two or more logic gates can be connected to produce a logic circuit with one or more outputs from two or more inputs. A logic circuit can process logical expressions and binary numbers.

When producing a truth table for a logic circuit:

- it is helpful to add a column for each intermediate output as well as for the final output
- as for a single logic gate with two inputs, a logic circuit with two inputs needs four rows.

Combinational logic circuits with three inputs

We only need to be able to produce a truth table for a logic circuit with a maximum of three inputs and six gates.

The truth table for a three-input logic circuit needs eight rows.

Designing simple logic circuits

Sometimes, it is cheaper to design and hard-wire a logic circuit for a simple automated system that only requires a fixed pattern of output depending on the current values of the inputs, than to program a microcontroller or computer.

We can use the words AND, OR, NOT, NAND and NAND as operators in a logical equation, such as L = (A AND B) OR NOT B. We use brackets to indicate that the logical operation within the brackets takes priority.

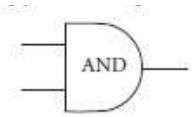
We can design a logic circuit to solve a written statement of a logical problem. First, we rewrite the statement using brackets to clarify the binary value of each variable and the priority of the logical operations. Then we can write the logical equation. From the logical equation, if not an earlier stage in the rewriting process, it should be possible to draw the required logic circuit and a truth table to confirm that it has the required behaviour.

Testing logic circuits

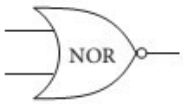
We have seen how to use a truth table to check whether a logic circuit has solved a given problem, rather as we use a trace table for dry running a flowchart or pseudo code algorithm. We can also check that a logic circuit solves the problem by building the circuit using logic simulation software or electronic circuitry, with appropriate attention to safety.

Practice Questions

Q 1) Complete the following truth table



INPUT 1	INPUT 2	OUTPUT
0	0	
0	1	
1	0	
1	1	



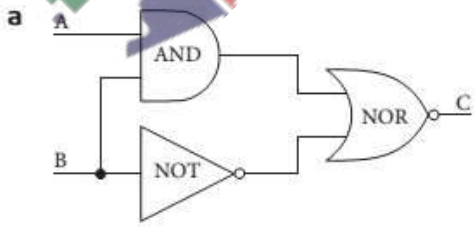
INPUT 1	INPUT 2	OUTPUT
0	0	
0	1	
1	0	
1	1	

Q 2) Draw the logic circuit required to fulfil the following statements:
a Output C = (NOT(A AND B)) AND (A OR B)

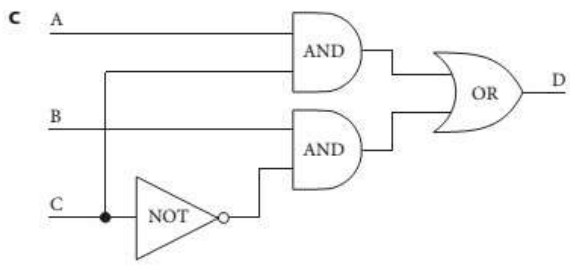
b Light (L) is **on** if Switch A is **on** OR (Switch B is **on** AND Input C is **off**.

Q 3) Copy and complete the truth tables for the following logic circuits:

a

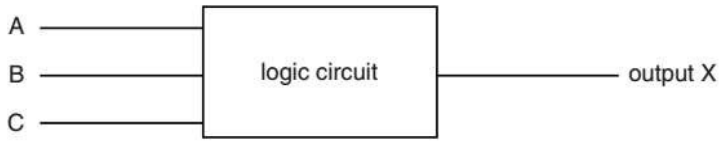


INPUT		Workspace	OUTPUT
A	B		C
0	0		
0	1		
1	0		
1	1		



A	B	C	Working	D
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

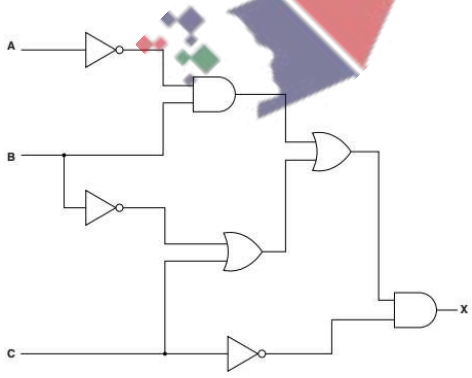
Q 4) Three digital sensors A, B and C are used to monitor a process. The outputs from the sensor s are used as the inputs to a logic circuit.
A signal, X, is output from the logic circuit:



Output, X, has a value of 1 if either of the following two conditions occur:
• sensor A outputs the value 1 OR sensor B outputs the value 0
• sensor B outputs the value 1 AND sensor C outputs the value 0
Draw a logic circuit to represent these conditions.

A	B	C	Working	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

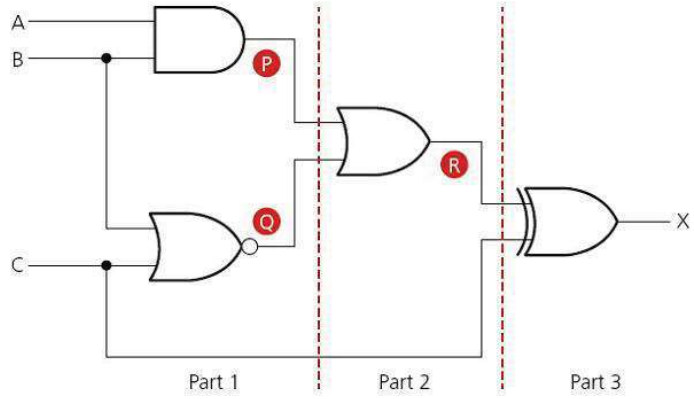
Q 5) Write a logic statement that describes the following logic circuit.



.....

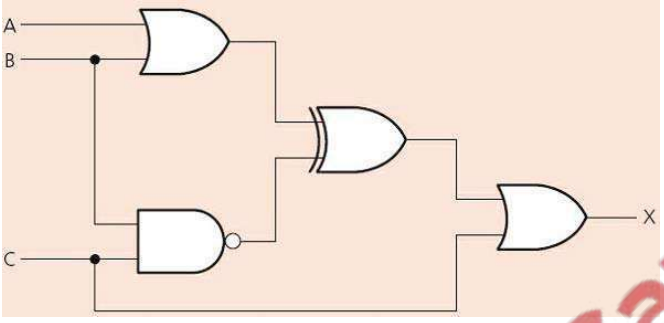
..... [3]

Q 6) Complete the truth table for the following logic circuit:



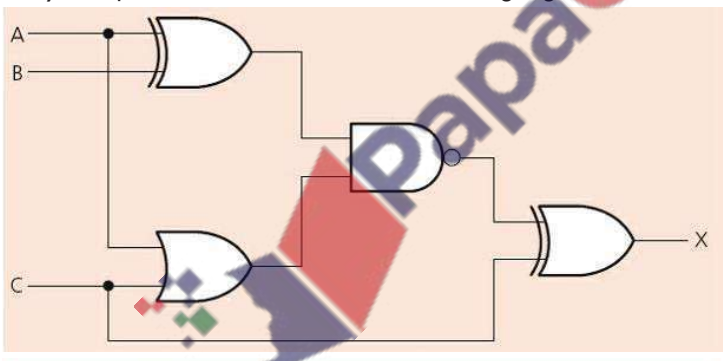
A	B	C		X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

Q 7) Complete the truth table for the following logic circuit:

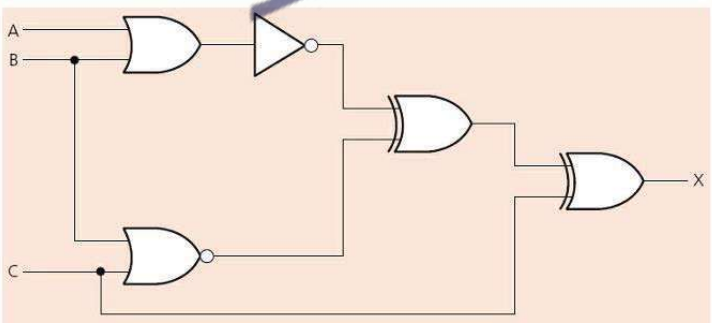


A	B	C		X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

Q 8) Complete the truth table for the following logic circuit:



A	B	C		X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		



A	B	C		X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

Quick Revision Questions

Q 3.1) Identify each of the following gates from truth table:

INPUT 1	INPUT 2	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	1

INPUT 1	INPUT 2	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

.....

INPUT 1	INPUT 2	OUTPUT
0	0	0
0	1	0
1	0	0
1	1	1

.....

INPUT 1	INPUT 2	OUTPUT
0	0	o
0	1	1
1	0	1
1	1	0

.....

INPUT 1	INPUT 2	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

.....

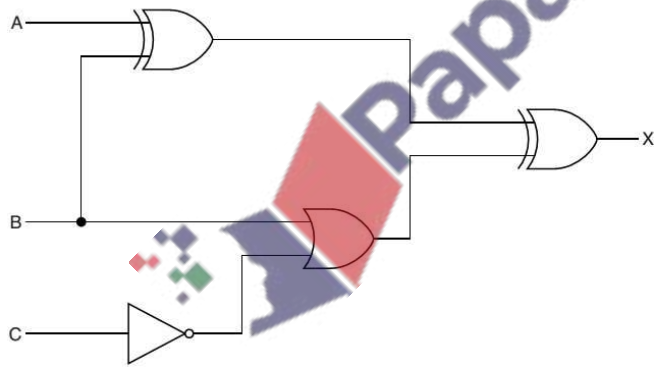
INPUT 2	OUTPUT
0	1
1	0

.....

.....

Q 3.2) Summer 2015 P11

3 (a) Complete the truth table for the following logic circuit:



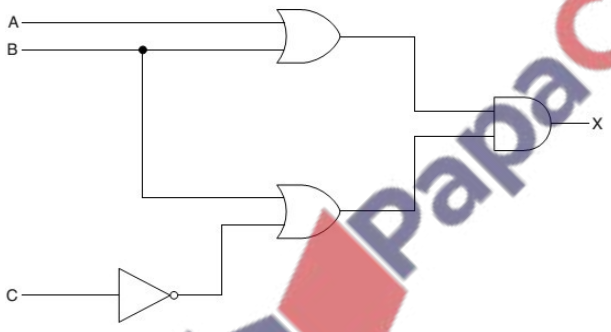
A	B	C	Workspace	X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

(b) Write the Boolean statement for the following logic statement:
X = 1 if ((A is **NOT** 1 **OR** B is 1) **AND** C is 1) **OR** (B is **NOT** 1 **AND** C is 1)

…… [3]

(c) Draw the logic circuit for the logic statement given in part b

(d) Write a logic statement which corresponds to the following logic circuit:



……

……

……[3]

Q 3.7a) A greenhouse control system has four input parameters (H, D, T, W) and two outputs (X, Y).

Parameter	Description of parameter	Binary value	Condition
H	Humidity	0	Too low
		1	Acceptable
D	Day	0	Night
		1	Day
T	Temperature	0	Too high
		1	Acceptable
W	Windows	0	Closed
		1	Open

The watering system turns on (X = 1) if:

either it is daytime **and** the temperature is too high

or the humidity is too low.

The fan turns on (Y = 1) if the temperature is too high **and** the windows are closed. Draw a logic circuit to represent the greenhouse control system. [6]

(b) Complete the truth table for the logic expression: **X** = NOT **A** AND (**B** NAND **C**) [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 3.8a) An alarm system (X) is enabled and disabled using either a switch (A) or a remote control (B).There are **two** infra-red sensors (C, D) and **one** door pressure sensor (E).

Parameter	Description of parameter	Binary value	Condition
A	Switch	1	Switch enabled
		0	Switch disabled
B	Remote control	1	Remote enabled
		0	Remote disabled
C	Infra-red sensor	1	Activated
		0	Not activated
D	Infra-red sensor	1	Activated
		0	Not activated
E	Door pressure sensor	1	Activated
		0	Not activated

The alarm sounds (X = 1) if the alarm is enabled **and** any one or more of the sensors is activated.

Draw a logic circuit to represent the alarm system.

[3]

(b) Complete the truth table for the logic expression: **X** = **A** OR (**B** XOR **C**) [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Draw a logic circuit corresponding to the logic statement: [3]

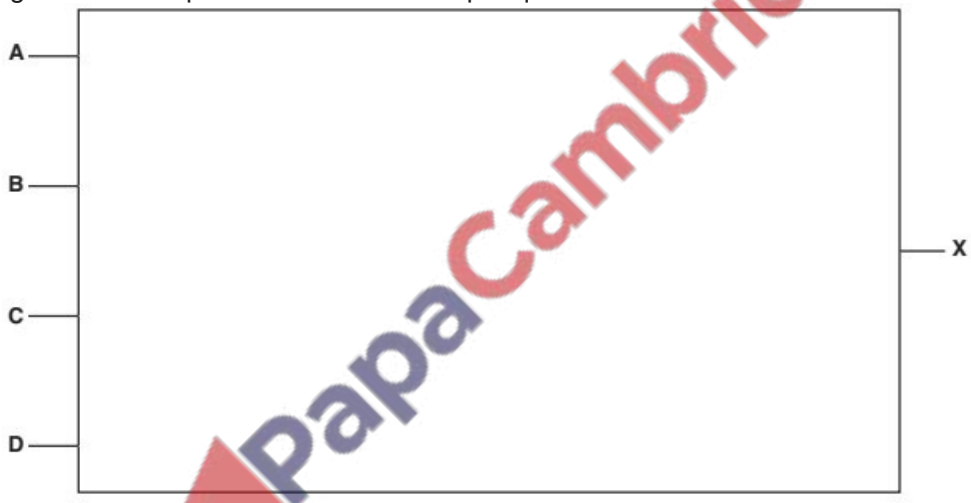
X = (**A** is ON OR **B** is ON **BUT NOT BOTH**) OR (NOT(**C** is ON AND **A** is ON))

Q 3.9a) A student needs to design a logic circuit to model the requirements for membership of a snooker club. Membership (X) depends on four criteria, as shown in the table:

Parameter	Description of parameter	Binary value	Condition
A	Over 18	1	True
		0	False
B	Recommended	1	True
		0	False
C	Full-time	1	True
		0	False
D	Retired	1	True
		0	False

Membership is approved (X = 1) if the person:
• is over the age of 18 **and** has been recommended by a pre-existing member **and**
• **either** is working full-time **or** is retired, **but not both.**

Draw a logic circuit to represent the membership requirements.



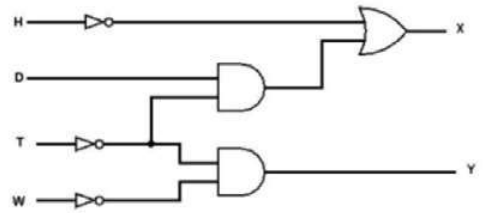
[3]

(b) Complete the truth table for the logic expression: **X** = (**A** XOR **B**) AND NOT **C** [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 3.7) Marking Scheme

1 mark for each gate with the correct inputs.
Final two gates must also have the correct output.

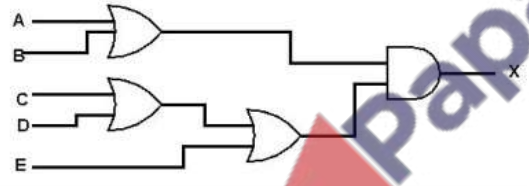


One mark for each pair of rows.

A	B	C	Working space	X
0	0	0		1
0	0	1		1
0	1	0		1
0	1	1		0
1	0	0		0
1	0	1		0
1	1	0		0
1	1	1		0

Q 3.8) Marking Scheme

1 mark per bullet:
- A OR B
- C OR D OR E
- Final AND

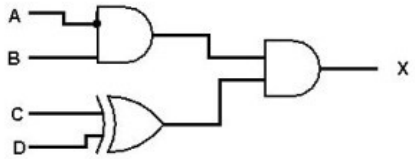


1 mark for each correct pair of rows

A	B	C	Working space	X
0	0	0		0
0	0	1		1
0	1	0		1
0	1	1		0
1	0	0		1
1	0	1		1
1	1	0		1
1	1	1		1

Q 3.9) Marking Scheme

1 mark per correct gate with correct inputs



1 mark for each correct pair of lines

A	B	C	Working space	X
0	0	0		0
0	0	1		0
0	1	0		1
0	1	1		0
1	0	0		1
1	0	1		0
1	1	0		0
1	1	1		0

Technical Update

Cambridge O Level
Computer Science 2210

For examination in June and November 2020.

From 2020, logic statements in the Paper 1 examination might not include the output and input values, such as 1 and 0. Therefore candidates must know how to interpret logic statements both with and without input and output values being written in the logic statement.

For example, the logic statement:

X = 1 if ((A is 1 OR B is 1) AND (A is 1 AND B is 1)) OR (C is NOT 1)

Can also be written as:

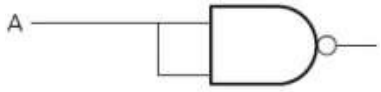
X = ((A OR B) AND (A AND B)) OR (NOT C)

Logic Building Block

It is possible to build up any logic gate, using NAND or NOR gates only.
NAND and NOR Gates can be used to build any other gates, and called 'logic building block'. It is cost effective for manufacturer to use a single gate to build any logic circuit.
For example, the AND, OR and NOT gates can be built from these gates as shown below:

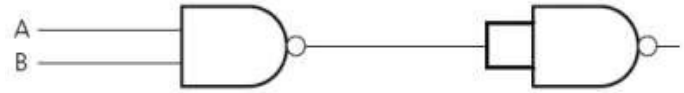
NAND as NOT:

If single input is given to NAND or NOT gate output will inverted

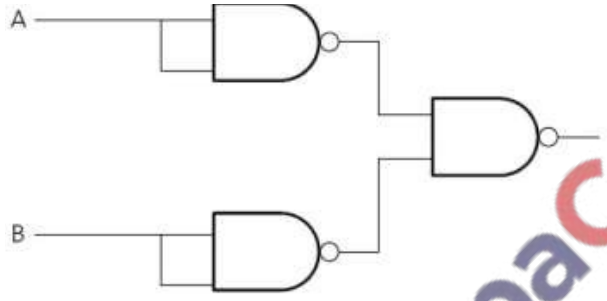


NAND as AND:

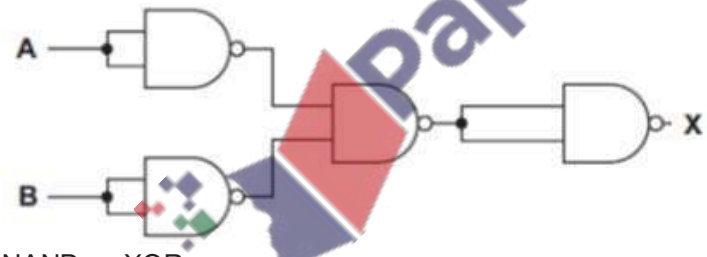
NAND on NAND will become AND



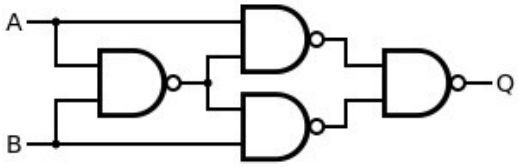
NAND as OR:



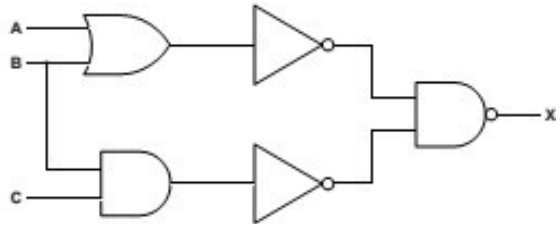
NAND as NOR



NAND as XOR

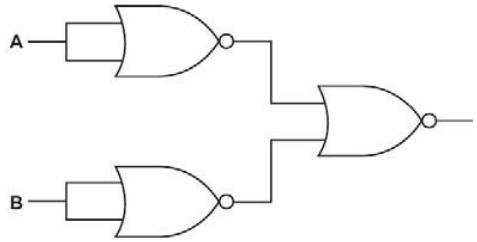


For example



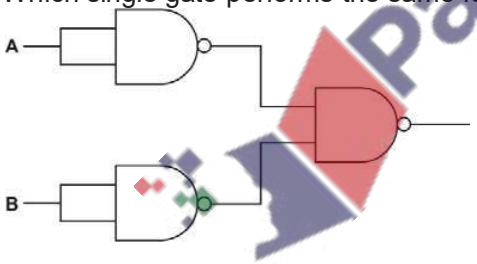
Re-draw the logic circuit shown opposite, using NAND and NOR gates only.

Complete the truth table for following circuits:



A	B	Working	X
0	0		
0	1		
1	0		
1	1		

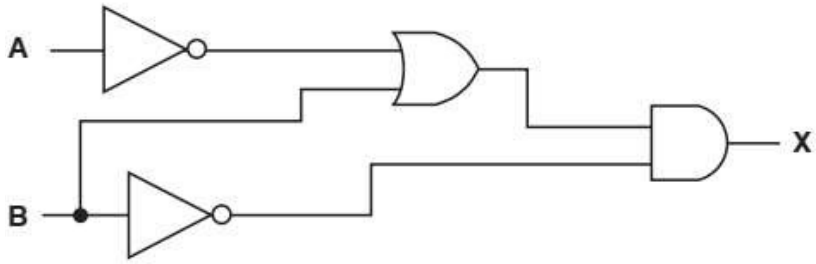
Which single gate performs the same function? ……



A	B	Working	X
0	0		
0	1		
1	0		
1	1		

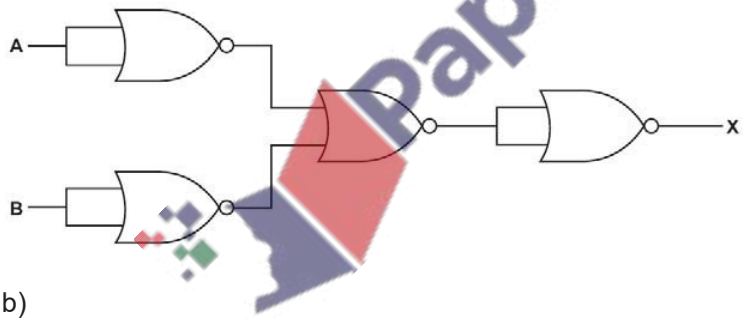
Which single gate performs the same function? ……

Simplification Logic Circuit:
Simplification means reducing the number of components in a logic circuit. As a result of simplification the cost of production can be less. This can also improve reliability and make it easier to trace faults if they occur.
The following logic circuit can be simplified to use only one gate.



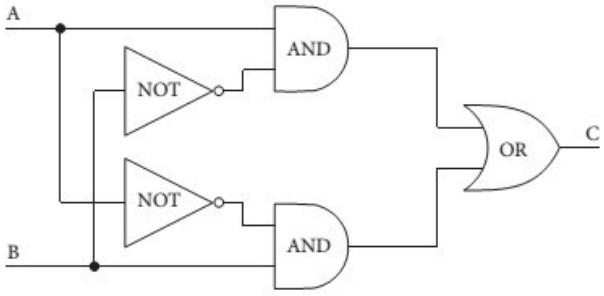
Give the name of this single gate.
..... [1]

Q 3.3) Show by drawing a truth table which single logic gate or what else has the same function as the logic circuit drawn in
a)



INPUT		Workspace	OUTPUT
A	B		X
0	0		
0	1		
1	0		
1	1		

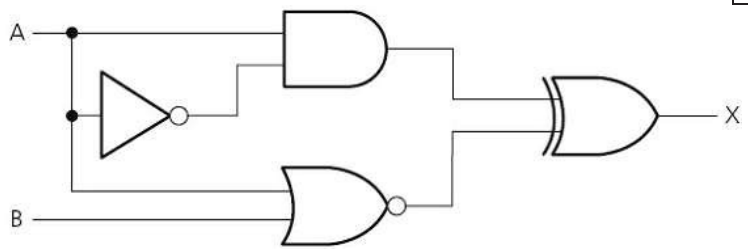
b)



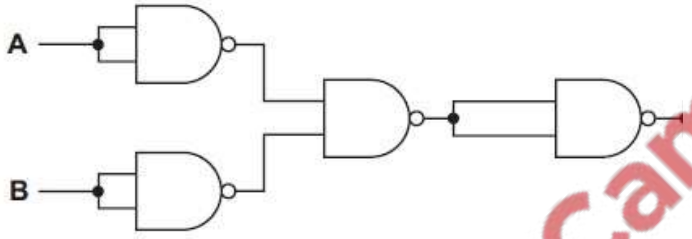
INPUT		Workspace	OUTPUT
A	B		C
0	0		
0	1		
1	0		
1	1		

c)

INPUT		Workspace	OUTPUT
A	B		X
0	0		
0	1		
1	0		
1	1		



d)



INPUT		Workspace	OUTPUT
A	B		C
0	0		
0	1		
1	0		
1	1		

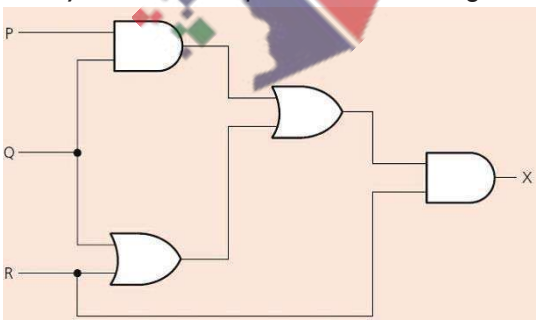
e) Explain why a single logic gate is often replaced by a logic circuit such as shown in part a, b, c and d.

.....

.....

.....[1]

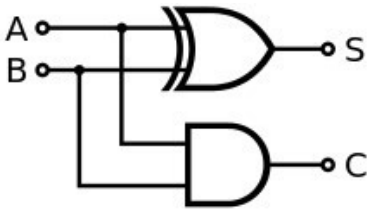
Q 3.4) What could replace the whole logic circuit?



INPUT			Workspace	
P	Q	R		X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

Multiple output:

Q 3.5) Multiple outputs can be obtained from a logic circuit. For example in the given logic circuit 2 outputs 'S' and 'C' are generated.



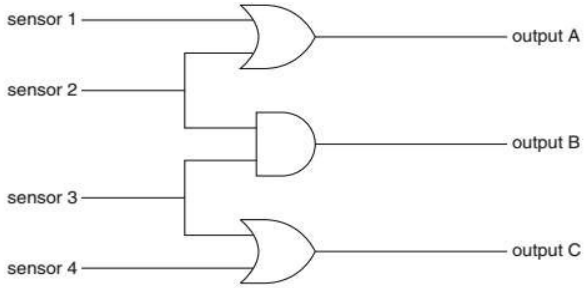
INPUT		OUTPUT	
A	B	S	C
0	0		
0	1		
1	0		
1	1		

Q 6) The following three logic statements define the light sequence:

- R = 1 IF (A is NOT 1)
- G = 1 IF (B is 1 AND C is 1)
- Y = 1 IF (A is 1 AND NOT (B is 1 AND C is 1))

Draw the logic circuit that directly combines ALL three of these logic statements and produces three outputs R, G and Y. [5]

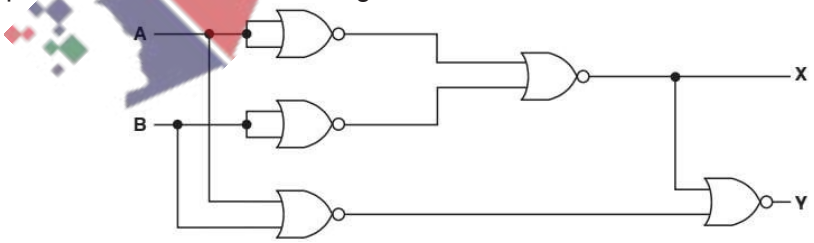
Q 7) Four sensors (numbered 1 to 4) produce binary output which controls the lights at a rock concert. The diagram shows how the sensors are connected:



Complete the truth table for this logic circuit. [4]

inputs				Outputs		
sensor 1	sensor 2	sensor 3	sensor 4	A	B	C
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

(b) (i) Complete the truth table for the logic circuit. [2]



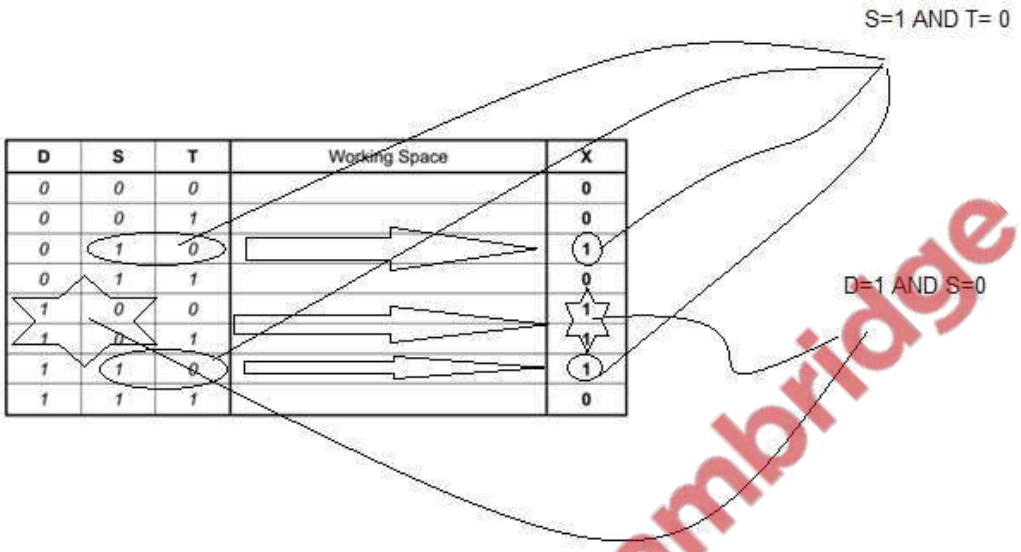
A	B	Working space	X	Y
0	0			
0	1			
1	0			
1	1			

Deriving Logic Statement and Drawing Logic Circuit from Given Truth Table.

Logic statement and circuit can be derived from truth table. Following are the steps:

1. Consider the output which are '1'
2. Find a condition of input when output is '1'
3. Check all above conditions produce output '1' or not.

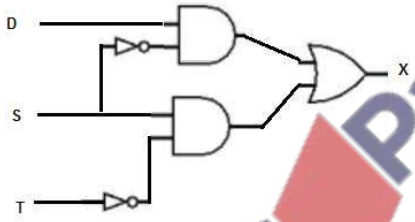
For example



So the logic statement will be

X=1 If (D=1 AND S=0) OR (S=1 AND T=0)

The Circuit diagram will be



Q 3.6) Write logic statement for the following truth table:

A	B	C	OUTPUT X
1	1	1	0
1	1	0	1
1	0	1	1
1	0	0	1
0	1	1	0
0	1	0	1
0	0	1	0
0	0	0	0

Candidate Example response

Example candidate response – high

6 A gas fire has a safety circuit made up of logic gates. It generates an alarm (X = 1) in response to certain conditions.

Input	Description	Binary value	Conditions
G	gas pressure	1	gas pressure is correct
		0	gas pressure is too high
C	carbon monoxide level	1	carbon monoxide level is correct
		0	carbon monoxide level is too high
L	gas leak detection	1	no gas leak is detected
		0	gas leak is detected

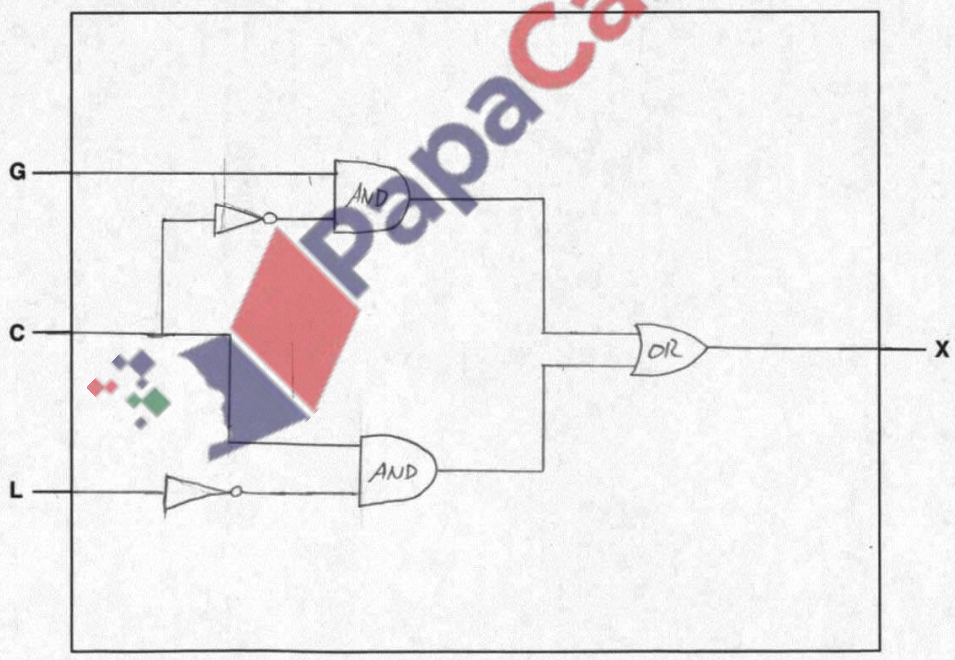
The output X = 1 is generated under the following conditions:

gas pressure is correct **AND** carbon monoxide level is too high

OR

carbon monoxide level is correct **AND** gas leak is detected

(a) Draw a logic circuit for this safety system.



[5]

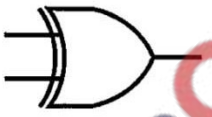
Example candidate response – high, continued

(b) Complete the truth table for the safety system.

G	C	L	Workspace $G \cdot \bar{C}$	Workspace $C \cdot \bar{L}$	Workspace $(G \cdot \bar{C}) + (C \cdot \bar{L})$	X
-0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	1	1	1
0	1	1	0	0	0	0
1	0	0	1	0	1	1
1	0	1	1	0	1	1
1	1	0	0	1	1	1
1	1	1	0	0	0	0

[4]

(c) Complete the truth table for the XOR gate:



A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

[1]

Examiner comment – high

In part **(a)** this candidate has drawn a neat and correct logic circuit. Candidates should make sure that gates are drawn clearly and accurately as this is what is assessed first.
In part **(b)** this candidate has correctly worked out the output for each section in the truth table. They have made good use of the working space available to do this; it is good practice for candidates to do so.
In part **(c)** this candidate has given the correct four outputs for the XOR gate.

Marks awarded for **(a)** = 5 out of 5
Marks awarded for **(b)** = 4 out of 4
Marks awarded for **(c)** = 1 out of 1

Total mark awarded = 10 out of 10

Example candidate response – middle

6 A gas fire has a safety circuit made up of logic gates. It generates an alarm (X = 1) in response to certain conditions.

Input	Description	Binary value	Conditions
G	gas pressure	1	gas pressure is correct
		0	gas pressure is too high
C	carbon monoxide level	1	carbon monoxide level is correct
		0	carbon monoxide level is too high
L	gas leak detection	1	no gas leak is detected
		0	gas leak is detected

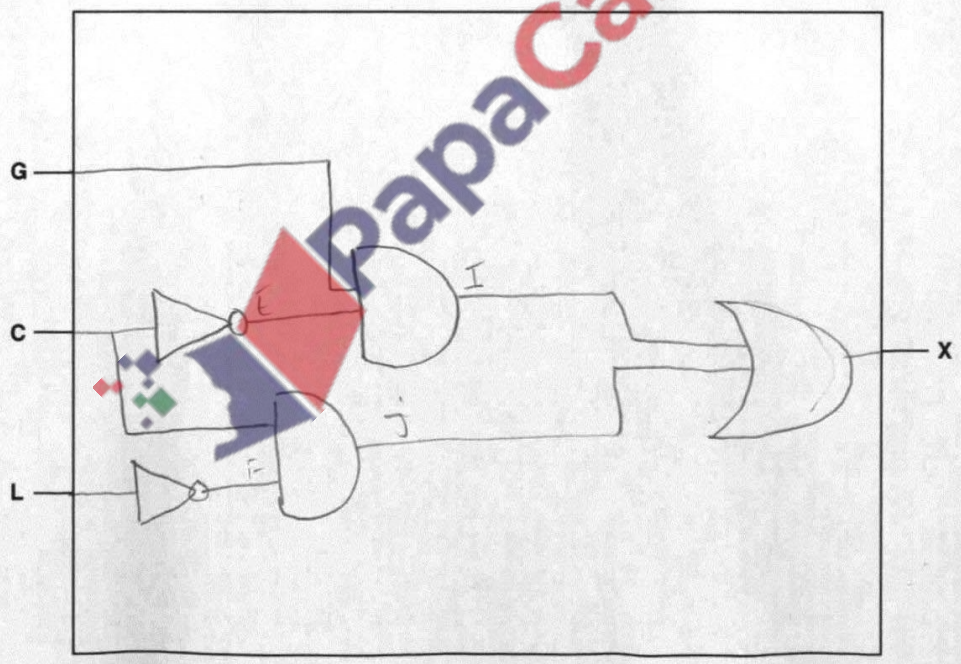
The output X = 1 is generated under the following conditions:

gas pressure is correct **AND** carbon monoxide level is too high

OR

carbon monoxide level is correct **AND** gas leak is detected

(a) Draw a logic circuit for this safety system.



[5]

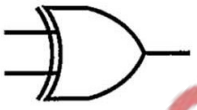
Example candidate response – middle, continued

(b) Complete the truth table for the safety system.

G	C	L	Workspace					X
0	0	0	1	1	0	0	0	0
0	0	1	1	0	0	0	0	0
0	1	0	0	1	0	0	0	0
0	1	1	0	0	0	1	1	1
1	0	0	1	1	0	0	0	0
1	0	1	1	0	0	0	0	0
1	1	0	0	1	1	0	1	1
1	1	1	0	0	1	1	1	1

[4]

(c) Complete the truth table for the XOR gate:



A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

0 1
1 0
1 0
1

[1]

Examiner comment – middle

In part **(a)** this candidate has drawn a neat and correct logic circuit. Candidates should make sure that gates are drawn clearly and accurately as this is what is assessed first.
In part **(b)** the candidate starts off well with one correct set of output. After this it appears that they begin to misunderstand the logic and cannot given any further correct sets of outputs.
In part **(c)** the candidate almost gets the correct answer, but is not quite right in their first output, so they do not get a mark.

Marks awarded for **(a)** = 5 out of 5
Marks awarded for **(b)** = 1 out of 4
Marks awarded for **(c)** = 0 out of 1

Total mark awarded = 6 out of 10

Example candidate response – low

6 A gas fire has a safety circuit made up of logic gates. It generates an alarm (X = 1) in response to certain conditions.

Input	Description	Binary value	Conditions
G	gas pressure	1	gas pressure is correct
		0	gas pressure is too high
C	carbon monoxide level	1	carbon monoxide level is correct
		0	carbon monoxide level is too high
L	gas leak detection	1	no gas leak is detected
		0	gas leak is detected

The output X = 1 is generated under the following conditions:

gas pressure is correct **AND** carbon monoxide level is too high

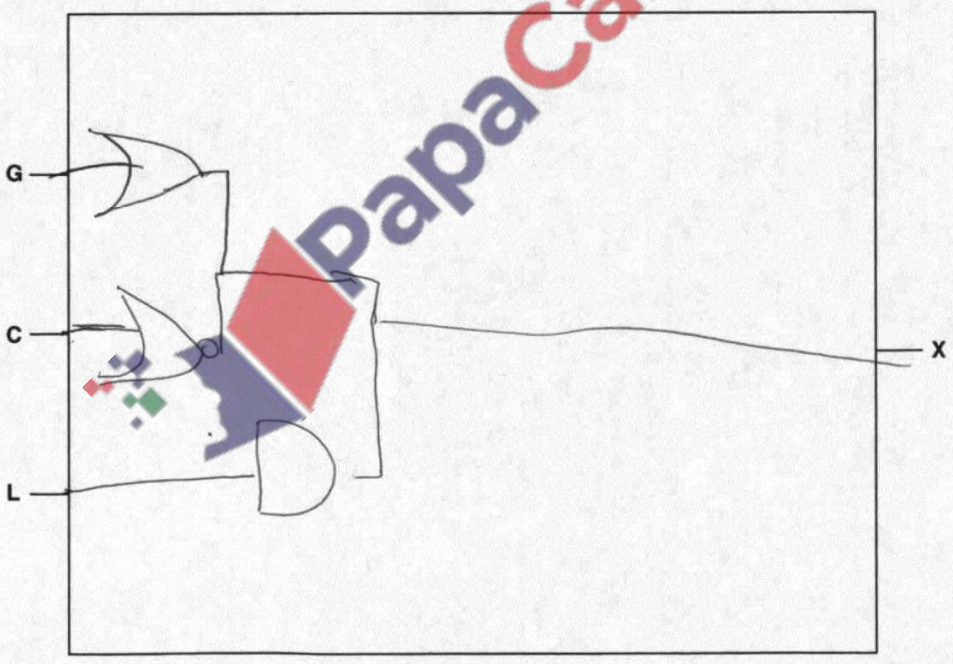
1 0

OR

carbon monoxide level is correct **AND** gas leak is detected

1 0

(a) Draw a logic circuit for this safety system.



[5]

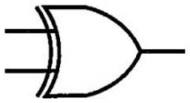
Example candidate response – low, continued

(b) Complete the truth table for the safety system.

G	C	L	Workspace	X
0	0	0		1
0	0	1		0
0	1	0		1
0	1	1		0
1	0	0		1
1	0	1		0
1	1	0		1
1	1	1		0

[4]

(c) Complete the truth table for the XOR gate:



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

[1]

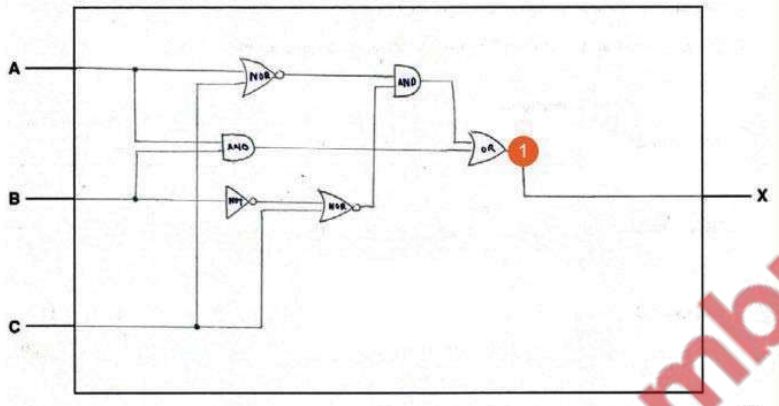
Examiner comment – low

In part **(a)** the candidate does not draw a logic circuit that will gain any marks. They also make a common error drawing one of their logic gates, the NOT gate. They miss off the small circular part at the tip of the gate, in the first gate. If candidates do this in their answer this cannot be classed as a NOT gate, as it is not drawn correctly.
In part **(b)** the candidate is able to make two sets of correct conversions.
In part **(c)** the candidate makes a common error with the last output. They have forgotten that if both inputs in an XOR gate are 1, the output will be 0 and not 1, like in an OR gate.

Marks awarded for **(a)** = 0 out of 5
Marks awarded for **(b)** = 2 out of 4
Marks awarded for **(c)** = 0 out of 1

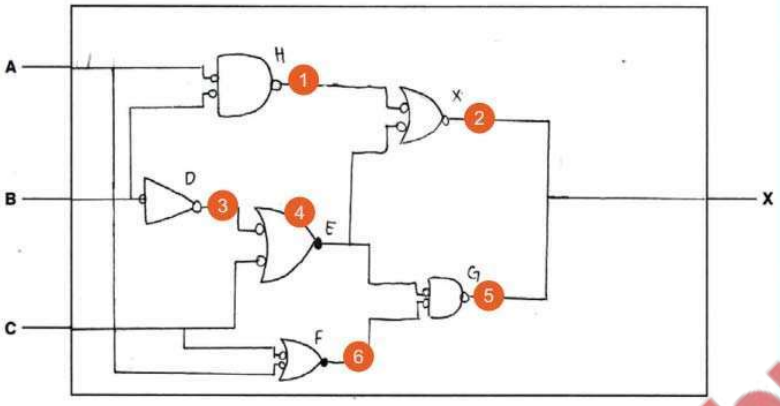
Total mark awarded = 2 out of 10

Question 8a

Example Candidate Response – high	Examiner Comments
8 Consider the logic statement: X = 1 if ((A is 1 NOR C is 1) AND (B is NOT 1 NOR C is 1)) OR (A is 1 AND B is 1) (a) Draw a logic circuit to match the given logic statement. Each logic gate used must have a maximum of **two** inputs. Do **not** attempt to simplify the logic statement.  [6]	1 A fully correct logic circuit is provided. **Total mark awarded = 6 out of 6**

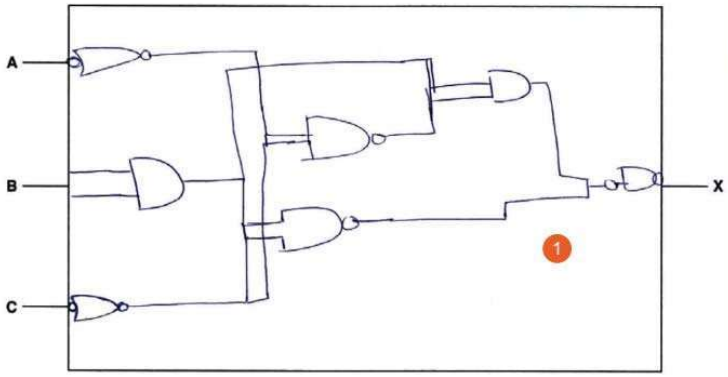
How the candidate could have improved their answer

The candidate provided a fully correct circuit. It would have been beneficial for the candidate to have drawn the gates slightly larger, to have made it easier to distinguish them.

Example Candidate Response – middle	Examiner Comments
8 Consider the logic statement: X = 1 if ((A is 1 NOR C is 1) AND (B is NOT 1 NOR C is 1)) OR (A is 1 AND B is 1) (a) Draw a logic circuit to match the given logic statement. Each logic gate used must have a maximum of **two** inputs. Do **not** attempt to simplify the logic statement.  [6]	1 This gate is not correct as the candidate includes a circle at the front of the gate, making a NAND gate, rather than an AND gate. 2 This gate is not correct. 3 This gate is correct and awarded a mark. It is advisable that the candidate does not include the small circles at the back of the gate. 4 This gate is awarded a mark. The candidate is given the benefit of the doubt for filling in the circle at the front of the gate. Candidates are advised not to do this. 5 This gate is not correct. 6 This gate is awarded a mark. The candidate is given the benefit of the doubt for filling in the circle at the front of the gate. Candidates are advised not to do this. **Total mark awarded = 3 out of 6**

How the candidate could have improved their answer

- It would have been beneficial for the candidate to have used the symbols provided in the syllabus. The use of the circles at the back of the gate could sometimes have made the gate have a different logic. Candidates should have avoided filling in circles at the front of gates.
- The candidate also had some incorrect logic gates in the circuit.

Example Candidate Response – low	Examiner Comments
8 Consider the logic statement: X = 1 if ((A is 1 NOR C is 1) AND (B is NOT 1 NOR C is 1)) OR (A is 1 AND B is 1) **(a)** Draw a logic circuit to match the given logic statement. Each logic gate used must have a maximum of **two** inputs. Do **not** attempt to simplify the logic statement.  [6]	1 The candidate doesn't provide any correct gates in the correct places. The NOT gates given are from A and C, but should only be from B. It is very unclear from the candidate's circuits which inputs are going into which gates. Candidates should make sure they draw circuits and gates as clear as they are able to. **Total mark awarded = 0 out of 6**

How the candidate could have improved their answer

The candidate demonstrated little understanding of creating a logic circuit. They made some fundamental errors, as well as incorrect logic gates. The candidate had tried to create two inputs to their first AND gate; that both came from input B. Inputs needed to come from two separate pathways. The candidate also had gates at the beginning and end of their circuit that only had one input. It was unclear what these gates were, but all gates except for NOT gates needed to have two inputs.

Common mistakes candidates made in this question

It was sometimes difficult to tell which gate a candidate had drawn. It would have been beneficial for candidates to have used the symbols given in the syllabus and ensured that they were clearly drawn.

Question 8b

Example Candidate Response – high	Examiner Comments
(b) Complete the truth table for the given logic statement. | A	B	C	Working space	X | |---|---|---|---|---| | 0 | 0 | 0 | | 0 | | 0 | 0 | 1 | | 0 | | 0 | 1 | 0 | | 1 | | 0 | 1 | 1 | | 0 | | 1 | 0 | 0 | | 0 | | 1 | 0 | 1 | | 0 | | 1 | 1 | 0 | | 1 | | 1 | 1 | 1 | | 1 | 1 [4]	1 The candidate provides eight correct outputs, gaining four marks. **Total mark awarded = 4 out of 4**

How the candidate could have improved their answer

The candidate has provided a fully correct truth table.

Example Candidate Response – middle

(b) Complete the truth table for the given logic statement.

A	B	C	Working space	X
0	0	0	~~Yes~~ No	0
0	0	1	Yes	1 ①
0	1	0	Yes	1
0	1	1	No	0
1	0	0	Yes	1 ②
1	0	1	No	0 ③
1	1	0	No	0
1	1	1	Yes	1 ④

[4]

Examiner Comments

1. This output is incorrect.
2. This output is incorrect.
3. This output is incorrect.
4. The candidate has five correct outputs, gaining them two marks.

Total mark awarded = 2 out of 4

How the candidate could have improved their answer

It was difficult to tell where the candidate had gone wrong in their logic workings as they had not provided their interim calculations. The working space in the table was provided to allow candidates to record their interim calculations, so they could keep track of the logic outputs.

Example Candidate Response – low

(b) Complete the truth table for the given logic statement.

A	B	C	Working space F A NOR C	D NOT B	E D NOR C	G F AND E	H A AND B	X H OR G	X
0	0	0	1	1	0	0	0	1	1
0	0	1	0	1	0	0	0	1	1
0	1	0	1	0	1	1	0	0	0
0	1	1	0	0	0	0	0	1	1
1	0	0	0	1	0	0	0	1	1
1	0	1	0	1	0	0	0	1	1
1	1	0	0	0	1	0	1	0	0
1	1	1	0	0	0	0	1	0	0 ①

[4]

Examiner Comments

1. The candidate hasn't managed to provide any correct outputs. They are all the reverse of what they should be.

Total mark awarded = 0 out of 4

How the candidate could have improved their answer

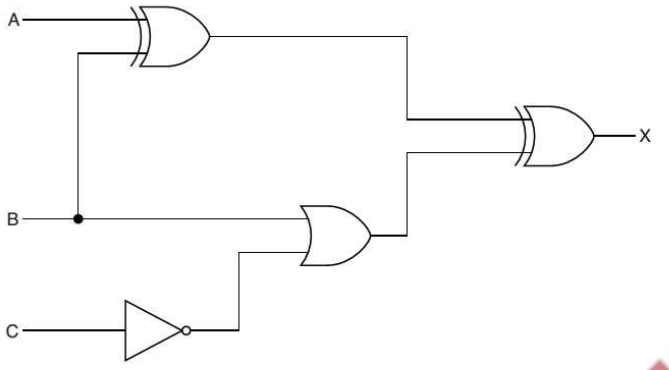
The candidate managed to provide the opposite output for each. This was likely because they had everything running through an AND gate and an OR gate at the end, rather than just the OR gate.

Common mistakes candidates made in this question

Candidates needed to have made sure that their answer was clear. Sometimes candidates used the working space and wrote their answer in the working space, rather than the correct output column. Candidates needed to make sure that their workings were in the working space, but that the final answer was in the output column.

Q 1) Summer 2015 P11

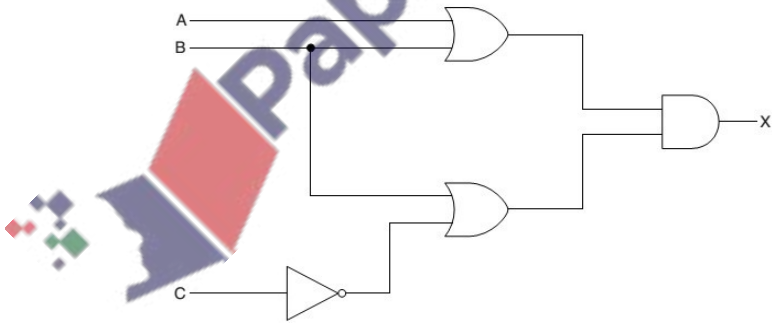
3 (a) Complete the truth table for the following logic circuit:



A	B	C	Workspace	X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

(b) Draw a logic circuit which corresponds to the following logic statement:
X = 1 if ((A is **NOT** 1 **OR** B is 1) **AND** C is 1) **OR** (B is **NOT** 1 **AND** C is 1)

(c) Write a logic statement which corresponds to the following logic circuit:



……

……

……[3]

Examiner's Comments on Question 3 (a), (b) and (c)

Many candidates gained most of the marks for this question, demonstrating a good standard of knowledge and application with logic gates.

In part (b), for some candidates' work, it was difficult to identify the difference between the AND gate and the OR gate. Candidates need to make sure that they draw the gates very clearly. For this question, candidates either understood the logic and provided an accurate circuit, or had little understanding of the logic and were unable to provide a circuit that gained any marks.

For part (c) many candidates gained at least two marks. Some candidates provided a description of the logic circuit rather than a logic statement and did not gain marks as a result.

Q 2) Summer 2015 P12

6 A gas fire has a safety circuit made up of logic gates. It generates an alarm (X = 1) in response to certain conditions.

Input	Description	Binary value	Conditions
G	gas pressure	1	gas pressure is correct
		0	gas pressure is too high
C	carbon monoxide level	1	carbon monoxide level is correct
		0	carbon monoxide level is too high
L	gas leak detection	1	no gas leak is detected
		0	gas leak is detected

The output X = 1 is generated under the following conditions:

gas pressure is correct **AND** carbon monoxide level is too high

OR

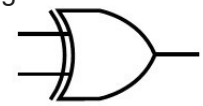
carbon monoxide level is correct **AND** gas leak is detected

(a) Draw a logic circuit for this safety system. [5]

(b) Complete the truth table for the safety system. [4]

G	C	L	Workspace	X
1	1	1		
1	1	0		
1	0	1		
1	0	0		
0	1	1		
0	1	0		
0	0	1		
0	0	0		

(c) Complete the truth table for the XOR gate:



A	B	C
0	0	
0	1	
1	0	
1	1	

Examiner's comments on Questions 6(a), 6(b) and 6(c)

Many candidates demonstrated a good level of knowledge of producing logic gates in part (a). Candidates just need to make sure that they draw the gates very clearly. They need to make sure that the small circle at the front of a NOT logic gate is included and is visible in order for it to be a valid NOT gate. The most common error was the emission of the NOT logic gates from the circuit.
In part (b) the full range of marks were awarded. Those candidates gaining higher marks normally correlated to a correct answer given in part (a).
In part (c) around 50% of candidates could correctly give the output of an XOR gate.

Q 6) Summer 2016 P11 & P13

5 A computer-controlled machine produces plastic sheets. The thickness of each sheet must be within a certain tolerance. The sheets are kept below 50 °C as they move over rollers at 10 metres per second.

Three parameters need to be monitored all the time.

Parameter	Description	Binary value	Conditions
D	sheet thickness	1	thickness of sheet in tolerance
		0	thickness of sheet out of tolerance
S	roller speed	1	roller speed = 10 metres/second
		0	roller speed <> 10 metres/second
T	temperature	1	temperature < 50 °C
		0	temperature >= 50 °C

An alarm, **X**, will sound if:

thickness is in tolerance AND (roller speed <> 10 metres/second OR temperature >= 50 °C)

OR

roller speed = 10 metres/second AND temperature >= 50 °C

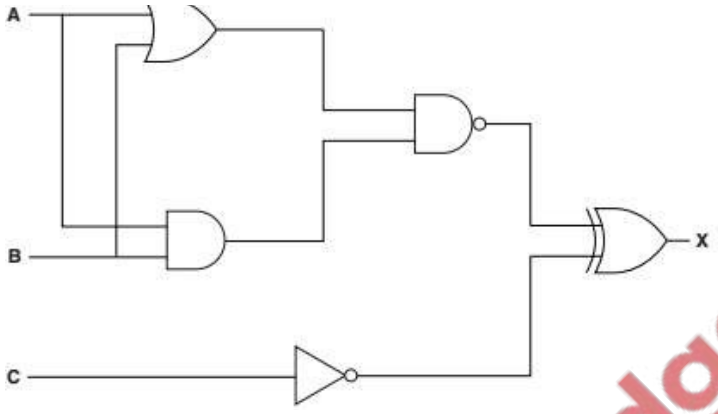
(a) Draw a logic circuit to represent the above monitoring system. [6]

(b) Complete the truth table for the monitoring system. [4]

D	S	T	Working Space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 7) Summer 2016 P12

7(a)



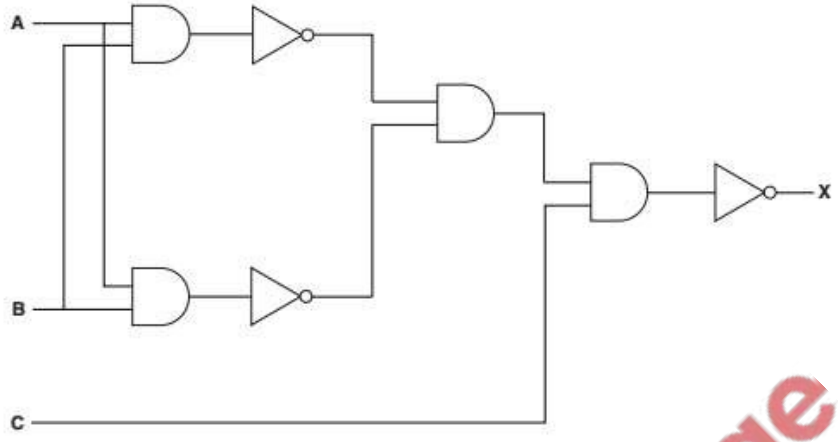
Complete the truth table for this logic circuit. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

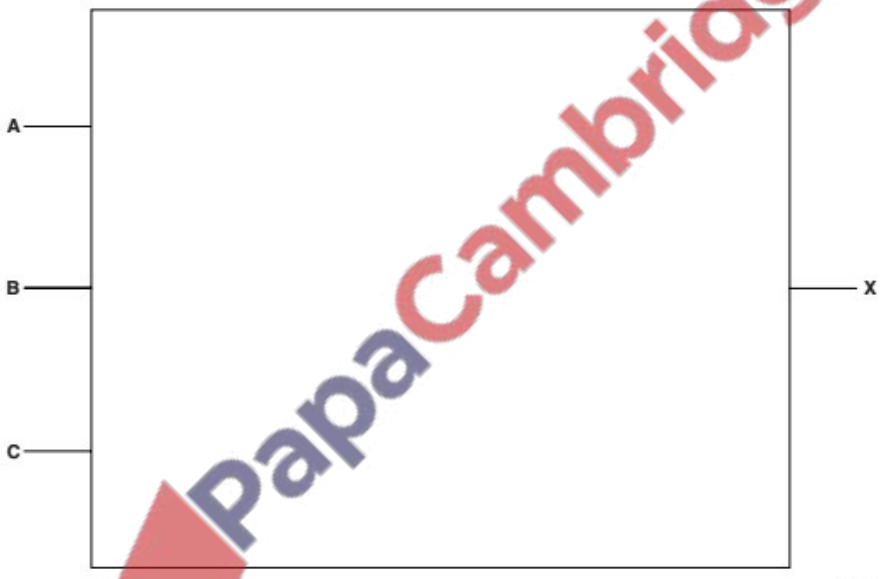
(b) Draw a logic circuit corresponding to the following logic statement:
X = 1 if ((A is 1 OR B is 1) AND (A is 1 AND B is 1)) OR (C is NOT 1)

[5]

(c) Re-draw the following logic circuit using NAND gates only.



Logic circuit re-drawn:



[4]

Examiner Report Question 7 (a), (b) and (c)

In part (a) most candidates were able to list the correct outputs.

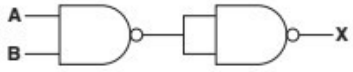
In part (b) many candidates were able to produce a correct logic circuit. Candidates created this in a variety of ways. Candidates are reminded to make sure that they accurate and clearly draw each logic gate. Some candidates did not draw a correct NOT logic gate, leaving the circle off the front. In some candidate's circuits, it was difficult to distinguish the difference between the AND gate and the OR gate.

In part (c) many candidates were able to gain some marks through the creation of a logic circuit using NAND gates. A common error was using an AND gate in the middle of the circuit, rather than two NAND gates. The question required only the use of NAND gates.

Q 8) Winter 2016 P12

7 (a) Complete the truth tables and name the single logic gate that could replace each logic circuit:

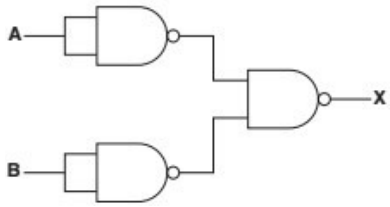
(i)



A	B	Working space	X
0	0		
0	1		
1	0		
1	1		

Single logic gate .....[3]

(ii)



A	B	Working space	X
0	0		
0	1		
1	0		
1	1		

Single logic gate .....[3]

(b) (i) Draw a logic circuit to represent the following logic statement:
X = 1 if (A = 1 AND B = 1) OR ((B = NOT 1) AND C = 1) [4]

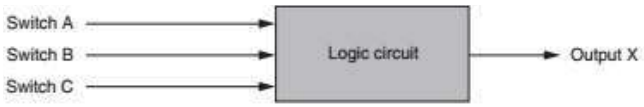
(ii) Complete the truth table for the logic statement in **part (b)(i)**. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Examiner Report
In parts **(a)(i)** and **(ii)** many candidates could complete the truth tables correctly, but were not able to state the correct single logic gate that the table represented.
In part **(b)(i)** many candidates could draw a correct logic circuit. A small number of candidates used circles to represent a logic gate. Candidates must ensure that they use the correct logic gate symbols, and that they are drawn clearly and accurately.
In part **(b)** many candidates could correctly complete the truth table.

Q 9) Winter 2016 P11& 13

5 Three switches, A, B and C, each send values of 0 or 1 to a logic circuit. Value X is output from the
logic circuit.



Output X has a value of 1 depending on the following conditions:

Switch A sends value 1 AND Switch B sends value 0
OR
Switch B sends value 1 AND Switch C sends value 0

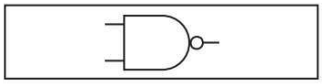
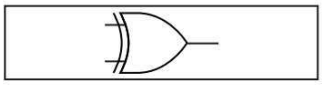
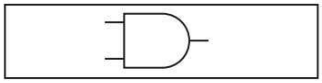
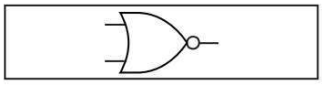
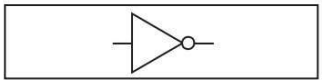
(a) Draw a logic circuit to represent the conditions above.

(b) Complete the truth table for the conditions given at the start of question 5. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 10) March 2017 India

2 The diagram below shows **five** logic gate symbols and **five** names.
Draw a line between each logic gate symbol and its correct name.

Logic Gate Symbol	Name
	AND
	NOT
	NOR
	XOR
	NAND

Examiner Report
Nearly all candidates correctly identified the five logic gates shown.

14 A system controls the flow of vehicles through a barrier based on three lights, A, B and C.
When a light is red, the signal is zero. When a light is green, the signal is one.
The barrier will open when the output X is one.
The barrier opens if either:

- light A is red and lights B and C are both green

or

- light A is green and lights B and C are both red

(a) Design a logic circuit for the system

[5]

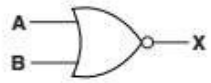
(b) Complete the truth table for the system given at the start of Question 14. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Examiner Report
(a) This was generally well answered.
(b) This was generally well answered.

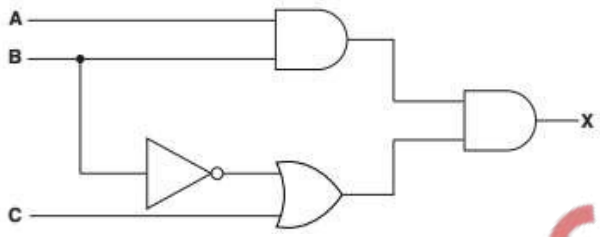
Q 11) Summer 2017 P11

10 (a) Complete the truth table for the NOR gate. [1]



A	B	Output (X)
0	0	
0	1	
1	0	
1	1	

(b) Write a logic statement that corresponds with the following logic circuit.



X = ... [3]

Examiner Comment on Q 10(a)

Many candidates provided the correct outputs for the logic gate.

Examiner Comment on Q 10(b)

Some candidates gave a correct statement. Some candidates did not use brackets in their statement andtherefore could only was awarded a single mark for the connecting AND. Candidates are reminded to makesure that they use brackets, where necessary, in their logic statements.

Q 12) Summer 2017 P12

10 For this logic statement:

X = 1 if ((A is 1 AND B is 1) OR (B is 1 AND C is NOT 1))

(a) Draw the logic circuit.

[4]

(b) Complete the truth table for the given logic statement. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Examiner Comment on Q 10(a)
Many candidates provided a correct logic circuit.
Examiner Comment on Q 10(b)
Many candidates provided a correct truth table.

Q 13) Winter 2017 P12

7 Draw a logic circuit to represent the logic statement: [7]

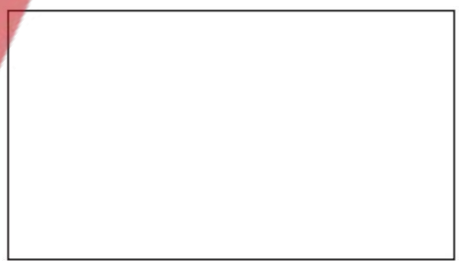
X = 1 if (A is NOT 1 AND B is 1) AND (A is NOT 1 AND C is NOT 1) OR (B is 1 AND C is 1)

Q 14) Winter 2017 P13

5 (a) Draw a logic circuit for the logic statement:

X = 1 if ((A is 1 AND B is 1) OR (A is NOT 1 AND C is 1)) [4]

(b) Draw the symbol for an XOR gate and explain the function of this logic gate.



Explanation .....

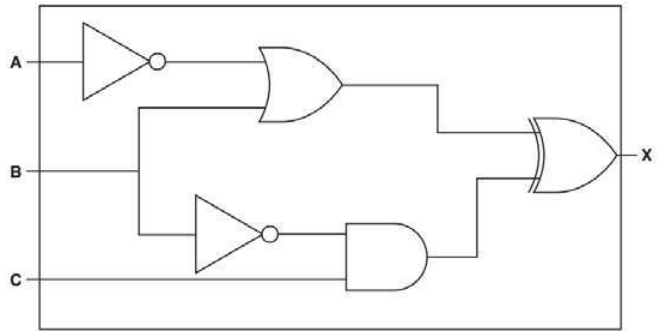
.....

.....

..... [5]

Q 15) March 2018 P12 (India)

7 (a) For this logic circuit:



Complete the truth table. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(b) For this logic statement:
X = 1 if (B is 1 OR C is NOT 1) AND ((A is NOT 1) AND (B is 1 OR C is 1))
Draw a logic circuit.

(c) Complete the truth table for the logic statement given in **part (b)**. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 16) Summer 2018 P11

6 Consider the logic statement:

X = 1 if ((A is NOT 1 OR B is 1) NOR C is 1) NAND ((A is 1 AND C is 1) NOR B is 1)

(a) Draw a logic circuit to represent the given logic statement. [6]

(b) Complete the truth table for the given logic statement. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 17) Summer 2018 P12

7 Consider the logic statement:

X = 1 if ((A is 1 AND B is NOT 1) NAND C is 1) XOR ((A is 1 AND C is 1) OR B is 1)

(a) Draw a logic circuit to represent the given logic statement. [6]

(b) Complete the truth table for the given logic statement. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 18) Winter 2018 P12

3 A greenhouse uses a system to monitor the conditions that plants need to grow.

The inputs to the system are:

Input	Binary value	Condition
W	1	Window is open
	0	Window is closed
T	1	Temperature >=26°C
	0	Temperature <26°C
H	1	Humidity >=50%
	0	Humidity <50%

The system will sound an alarm when certain conditions are detected.

Alarm (X) will sound (=1) when:

window is closed and temperature >=26°C

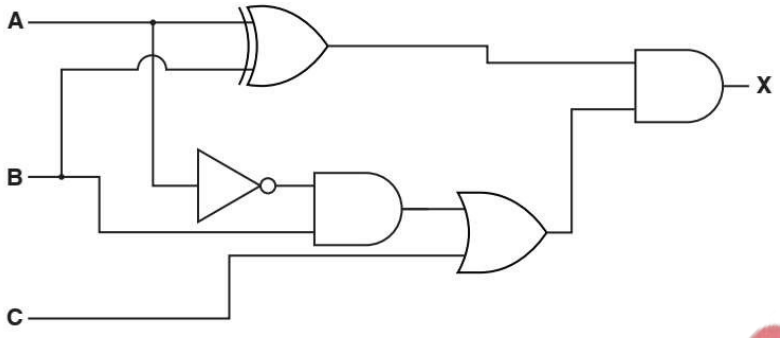
or

temperature <26°C and humidity >=50%

Draw a logic circuit to represent the system. [5]

Q 19) Winter 2018 P13

10 A logic circuit is shown:



(a) Complete the truth table for the given logic circuit. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(b) Draw a logic circuit corresponding to the logic statement:

X = 1 if ((A is 1 AND B is 1) AND (A is 1 OR C is NOT 1)) OR (B is 1 AND C is NOT 1) [6]

Q 20) March 2019 P12

5 Consider the following logic statement:

X = 1 if ((A is 1 NAND C is 1) NOR A is NOT 1) OR (B is 1 AND C is NOT 1)

(a) Draw a logic circuit that represents the given logic statement. Your logic gates must have a maximum of two inputs. Do **not** simplify the logic statement. [6]

(b) Complete the truth table for the given logic statement. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 21) Summer 2019 P11

2 Rajesh creates a logic circuit.

He uses three different logic gates in his circuit. Each logic gate has a maximum of **two** inputs.

He describes the logic of each gate.

(a) "The only time the output will be 1 is when both inputs are 1."

State the single logic gate .....

Draw the single logic gate: [2]

(b) "The only time the output will be 1 is when both inputs are 0."

State the single logic gate .....

Draw the single logic gate: [2]

(c) "The only time the output will be 0 is when both inputs are 1."

State the single logic gate .....

Draw the single logic gate: [2]

Q 22) Summer 2019 P12

8 Consider the logic statement:

X = 1 if ((A is 1 NOR C is 1) AND (B is NOT 1 NOR C is 1)) OR (A is 1 AND B is 1)

(a) Draw a logic circuit to match the given logic statement. Each logic gate used must have a maximum of **two** inputs. Do **not** attempt to simplify the logic statement.

[6]

(b) Complete the truth table for the given logic statement. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 23) Winter 2019 P13

4 A factory that manufactures cleaning products has a system that monitors conditions throughout the manufacturing process. The inputs to the system are:

Input	Binary value	Condition
A	1	pH > 7
	0	pH < = 7
T	1	Temperature < 35°C
	0	Temperature > = 35°C
P	1	Pressure > = 80%
	0	Pressure < 80%

(a) The system will sound an alarm (**X**) when certain conditions are detected.

The alarm will sound when:

The pressure > = 80% and the temperature > = 35°C

or

• The temperature < 35°C and the pH > 7

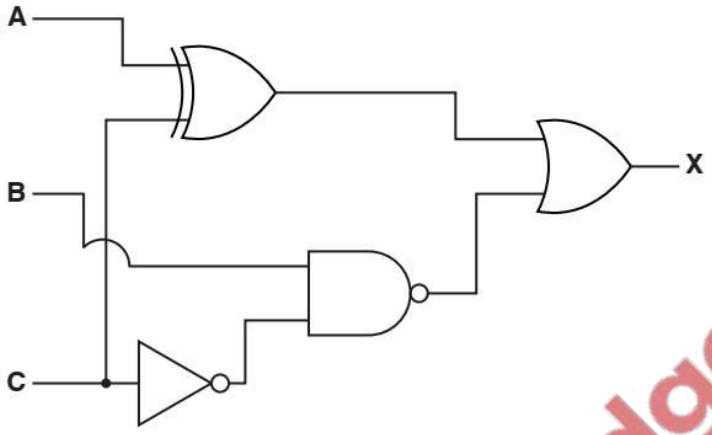
Draw a logic circuit to represent the alarm system in the factory. Each logic gate must have a maximum of two inputs. [4]

(b) Complete the truth table for the given logic problem. [4]

A	T	P	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 24) Winter 2019 P12

8 Consider the logic circuit:



(a) Write a logic statement to match the given logic circuit.

..... [3]

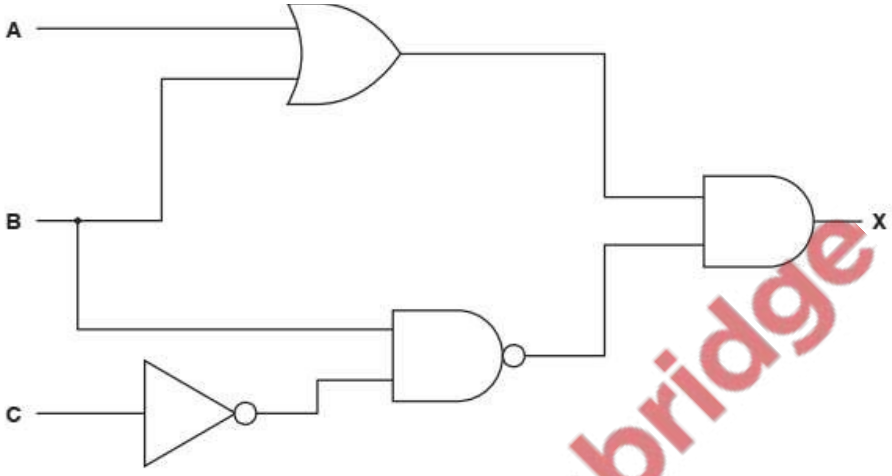
(b) Complete the truth table for the given logic circuit. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 25) March 20 P12

6 (a) Complete the truth table for the given logic circuit. [4]

Do **not** attempt to simplify the logic circuit.



A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(b) A water control system uses a switch and two pressure sensors.

The outputs of the switch and sensors are shown in the table.

Sensor or Switch	Output of 1	Output of 0
Switch (**S1**)	On	Off
Pressure Sensor (**P1**)	>= 3	< 3
Pressure Sensor (**P2**)	>= 3	< 3

Create a logic circuit that will produce an output (**X**) of 1 when:

The switch **S1** is on

and

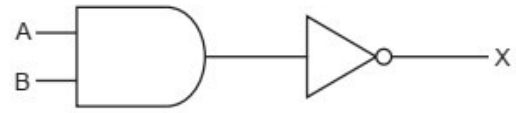
either P1 is less than 3 **or P2** is less than 3, **but not both**.

All logic gates used must have a maximum of two inputs. [4]

Q 26) Summer 20 P12

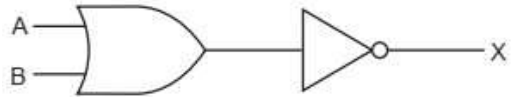
4 (a) Identify the name **and** draw the **single** logic gate that can replace the given logic circuits.

(i)



Name of gate: …… Drawing of gate: [2]

(ii)



Name of gate: …… Drawing of gate: [2]

(b) Complete the truth table for the given logic statement: [4]

X = (((**A** OR **C**) AND (NOT **A** AND NOT **C**)) XOR **B**)

A	**B**	**C**	Working space	**X**
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 27) 15a Summer 20 P11

2 Consider the logic statement:

X = (((**A** NAND **B**) OR (**B** XOR **C**)) AND NOT **C**)

(a) Draw a logic circuit to match the given logic statement.
All logic gates must have a maximum of **two** inputs. Do **not** attempt to simplify the logic statement. [5]

(b) Complete the truth table to represent the given logic statement. [4]

A	**B**	**C**	Working space	**X**
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 28) Winter 20 P12

4 Consider the logic statement:

X = (((**A** NAND **B**) NOR (**B** AND **C**)) OR **C**)

(a) Draw a logic circuit to match the given logic statement.

All logic gates must have a maximum of **two** inputs. Do **not** attempt to simplify the logic statement. [4]

(b) Complete the truth table for the given logic statement. [4]

A	**B**	**C**	Working space	**X**
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 29) Winter 20 P13

10 Consider the following logic statement:
X = ((**B** AND NOT **A**) XOR (**A** OR **C**))
(a) Draw a logic circuit to match the given logic statement.
All logic gates must have a maximum of **two** inputs. Do **not** attempt to simplify the logic statement. [4]

(b) Complete the truth table for the given logic statement. [4]

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Q 30) March 20 P12

5 Computers use logic gates.
(a) State the **single** logic gate that produces each truth table. [3]

Truth table			Logic gate
A	B	Output	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

(b) An aeroplane has a warning system that monitors the height of the aeroplane above the ground, whether the aeroplane is ascending or descending, and the speed of the aeroplane.

Input	Binary value	Condition
Height **(H)**	1	Height is less than 500 metres
	0	Height is greater than or equal to 500 metres
Ascending or Descending **(A)**	1	Aeroplane is ascending or in level flight
	0	Aeroplane is descending
Speed **(S)**	1	Speed is less than or equal to 470 knots
	0	Speed is greater than 470 knots

The warning system will produce an output of 1 that will sound an alarm (W) when either of these condition s apply:

Height is less than 500 metres and the aeroplane is descending

Or

The aeroplane is descending and speed is greater than 470 knots

Draw a logic circuit to represent the warning system. [5]

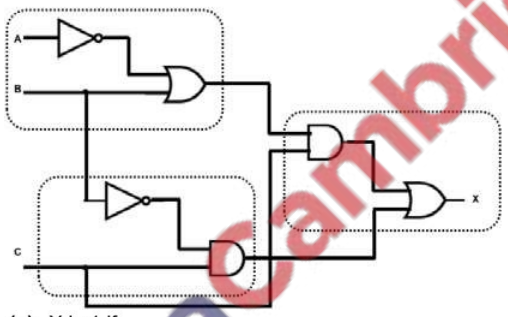
Marking Scheme

Q 1) Summer 2015 P11

3 (a)

A	B	C	Working	X
0	0	0		1
0	0	1		0
0	1	0		0
0	1	1		0
1	0	0		0
1	0	1		1
1	1	0		1
1	1	1		1

(b) 1 mark per dotted section



(c) X is 1 if:

(A is 1 OR B is 1)

AND

(B is 1 OR C is NOT 1)

accept equivalent ways of writing this:

e.g. (A OR B = 1) AND (B OR NOT C = 1)

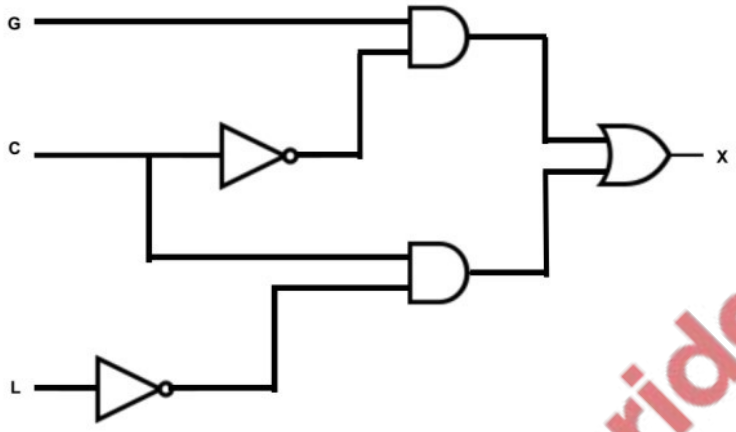
e.g. (A OR B) AND (B OR NOT C)

e.g. $(A + B)(B + \overline{C})$

Q 2) Summer 2015 P12

Page 7	Mark Scheme	Syllabus	Paper
	Cambridge O Level – May/June 2015	2210	12

6 (a) 1 mark per correct logic gate, correctly connected



[5]

(b)

G	C	L	Workspace	X	
0	0	0		0	1 mark
0	0	1		0	
0	1	0		1	1 mark
0	1	1		0	
1	0	0		1	1 mark
1	0	1		1	
1	1	0		1	1 mark
1	1	1		0	

[4]

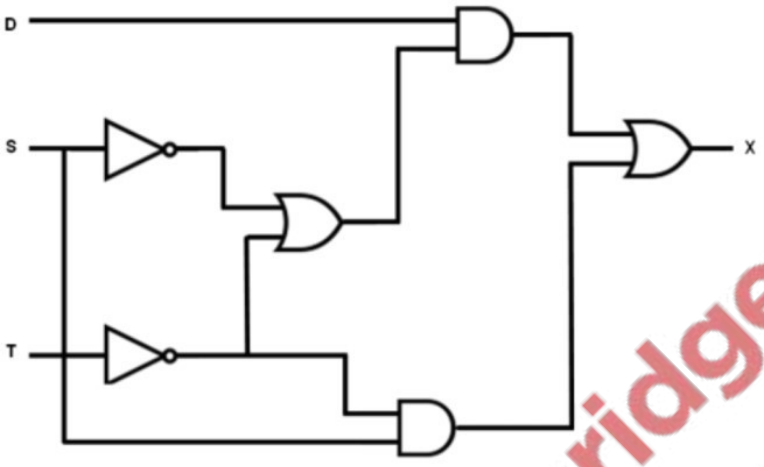
(c) 1 mark for correctly completed truth table

A	*B*	*C*
0	*0*	**0**
0	*1*	**1**
1	*0*	**1**
1	*1*	**0**

Q 6) Summer 2016 P11 & P13

Page 5	Mark Scheme	Syllabus	Paper
	Cambridge O Level – May/June 2016	2210	11

5 (a) **1** mark for each correct gate, with correct source of input(s)



[6]

(b)

D	S	T	Working Space	X
0	*0*	*0*		**0**
0	*0*	*1*		**0**
0	*1*	*0*		**1**
0	*1*	*1*		**0**
1	*0*	*0*		**1**
1	*0*	*1*		**1**
1	*1*	*0*		**1**
1	*1*	*1*		**0**

4 marks for 8 correct X bits
3 marks for 6 correct X bits
2 marks for 4 correct X bits
1 mark for 2 correct X bits

[4]

Q 7) Summer 2016 P12

Page 6	Mark Scheme	Syllabus	Paper
	Cambridge IGCSE – May/June 2016	0478	12

7 (a)

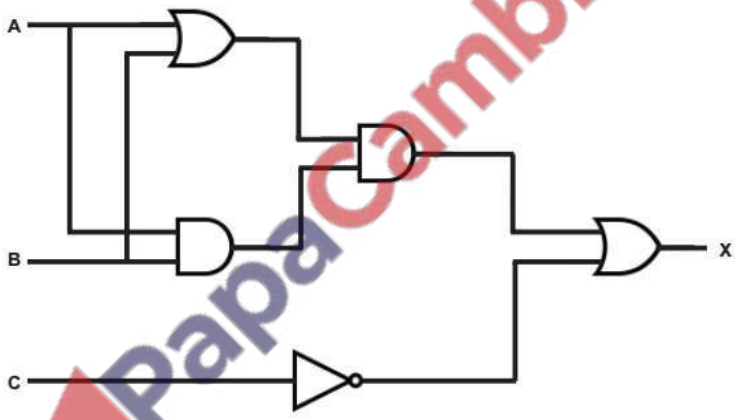
A	B	C	Working space	X
0	*0*	*0*		**0**
0	*0*	*1*		**1**
0	*1*	*0*		**0**
0	*1*	*1*		**1**
1	*0*	*0*		**0**
1	*0*	*1*		**1**
1	*1*	*0*		**1**
1	*1*	*1*		**0**

4 marks for 8 correct X bits
3 marks for 6 correct X bits
2 marks for 4 correct X bits
1 mark for 2 correct X bits

[4]

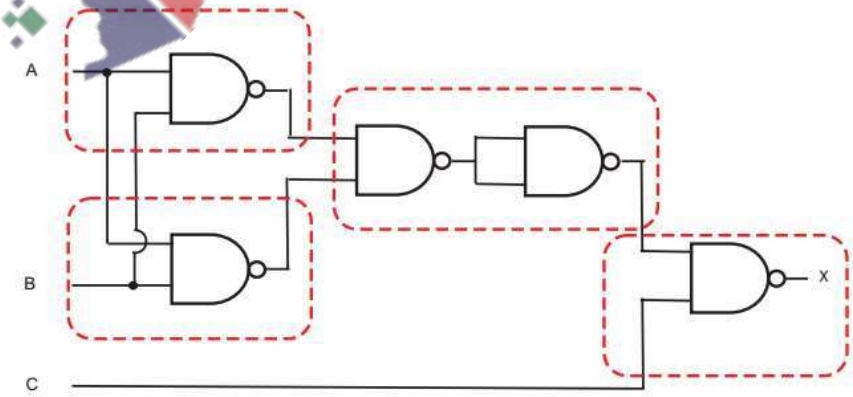
Page 7	Mark Scheme	Syllabus	Paper
	Cambridge IGCSE – May/June 2016	0478	12

(b) **1** mark for each correct gate with correct source of input



[5]

(c) Each dotted area is **1** mark



[4]

Q 8) Winter 2016 P12

Page 6	Mark Scheme	Syllabus	Paper
	Cambridge IGCSE – October/November 2016	0478	12

7 (a) (i) 2 marks for 4 correct outputs,
1 mark for 2 correct outputs

1 mark for correct gate

A	B	Working space	X
0	*0*		0
0	*1*		0
1	*0*		0
1	*1*		1

AND gate

[3]

(ii) 2 marks for 4 correct outputs
1 mark for 2 correct outputs

1 mark for correct gate

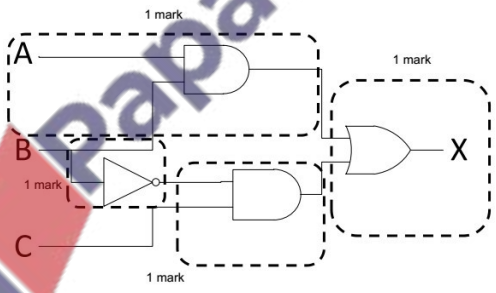
A	B	Working space	X
0	*0*		0
0	*1*		1
1	*0*		1
1	*1*		1

OR gate

[3]

Page 7	Mark Scheme	Syllabus	Paper
	Cambridge IGCSE – October/November 2016	0478	12

(b)(i) 1 mark per correct section.



[4]

(ii) 4 marks for 8 correct outputs
3 marks for 6 correct outputs
2 marks for 4 correct outputs
1 mark for 2 correct outputs

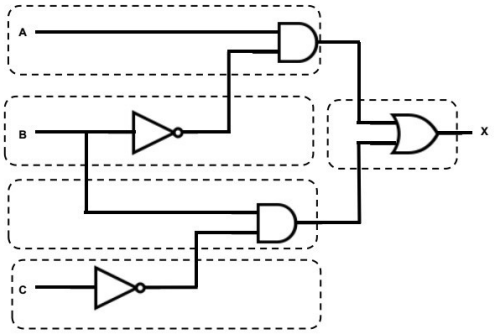
A	B	C	Working space	X
0	*0*	*0*		0
0	*0*	*1*		1
0	*1*	*0*		0
0	*1*	*1*		0
1	*0*	*0*		0
1	*0*	*1*		1
1	*1*	*0*		1
1	*1*	*1*		1

[4]

Q 9) Winter 2016 P11& 13

Page 5	Mark Scheme	Syllabus	Paper
	Cambridge IGCSE – October/November 2016	0478	13

5 **(a)** 1 mark per correct section.



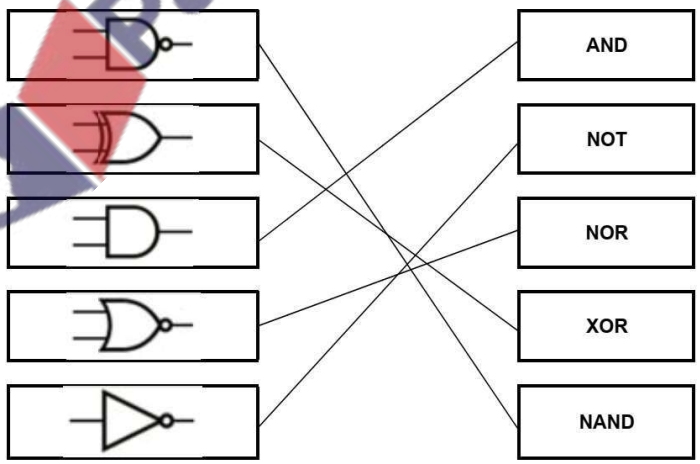
[5]

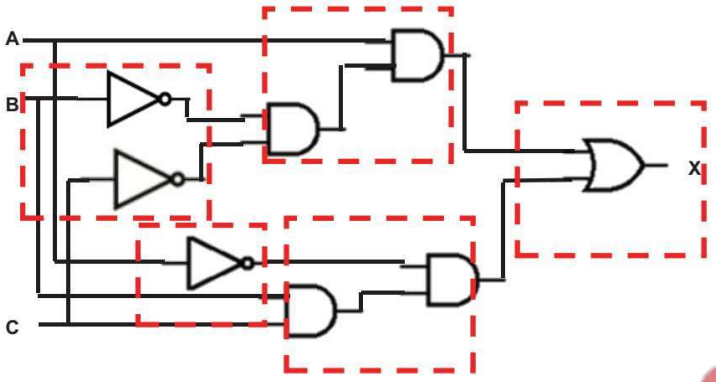
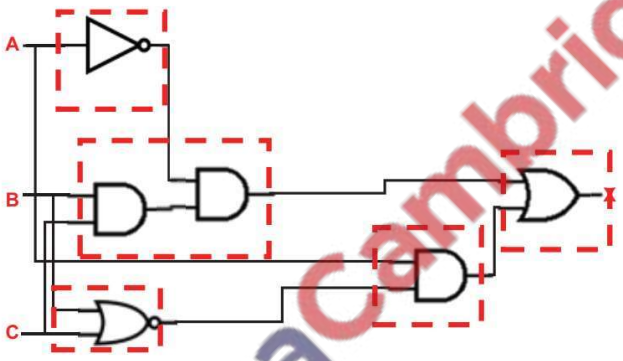
(b) 4 marks for 8 correct values
3 marks for 6 correct values
2 marks for 4 correct values
1 mark for 2 correct values

A	B	C	Working space	X
0	0	0		0
0	0	1		0
0	1	0		1
0	1	1		0
1	0	0		1
1	0	1		1
1	1	0		1
1	1	1		0

[4]

Q 10) March 2017 India

Question	Answer	Marks
2	1 mark for each correctly drawn line to a maximum of 4. **Logic Gate Symbol** / **Name**  AND NOT NOR XOR NAND	**4**

Question	Answer	Marks
14(a)	1 mark for each correct indicated area.  This is one example, many others exist. Alternative example  	5

Question	Answer	Marks
14(b)	4 marks for 8 correct bits 3 marks for 6 correct bits 2 marks for 4 correct bits 1 mark for 2 correct bits	4

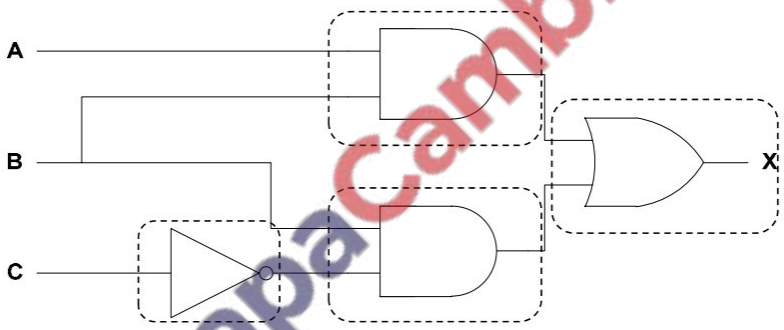
A	*B*	*C*	X
0	*0*	*0*	**0**
0	*0*	*1*	**0**
0	*1*	*0*	**0**
0	*1*	*1*	**1**
1	*0*	*0*	**1**
1	*0*	*1*	**0**
1	*1*	*0*	**0**
1	*1*	*1*	**0**

Q 11) Summer 2017 P11

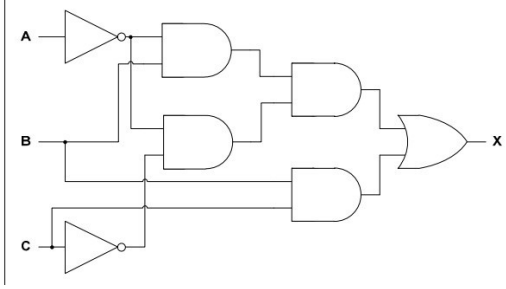
<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>10(a)</td><td>1 mark for four correct outputs only
<table><tr><th>A</th><th>B</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table></td><td>1</td></tr>
<tr><td>10(b)</td><td>1 mark for each correct section of the statement

∞ (A AND B)
∞ AND
∞ (C OR NOT B)</td><td>3</td></tr>
</table>

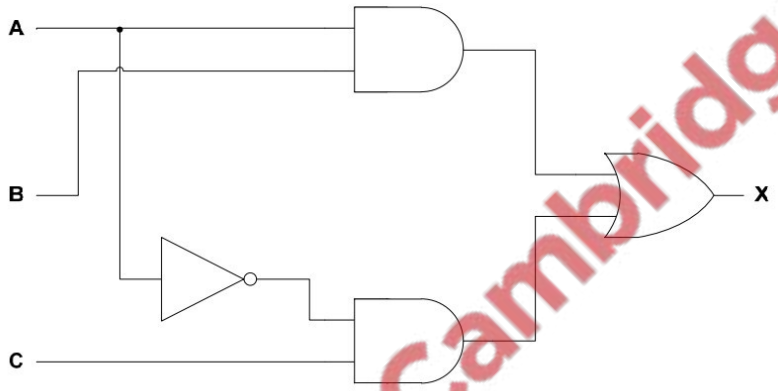
Q 12) Summer 2017 P12

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>10(a)</td><td>1 mark for each correct gate, with the correct input(s)
 
</td><td>4</td></tr>
<tr><td>10(b)</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>
4 marks for 8 correct outputs
3 marks for 6 or 7 correct outputs
2 marks for 4 or 5 correct outputs
1 mark for 2 or 3 correct outputs</td><td>4</td></tr>
</table>

Q 13) Winter 2017 P12

7	1 mark for each correct logic gate with the correct input(s) 	7

Q 14) Winter 2017 P13

Question	Answer	Marks
5(a)	1 mark for each correct logic gate 	4

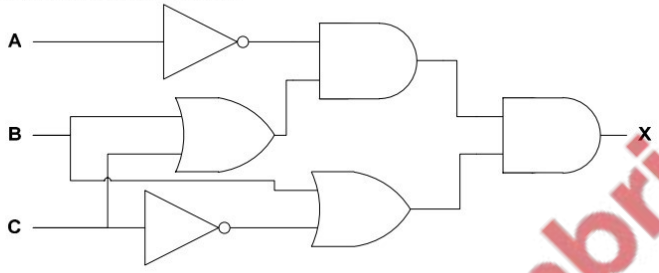
Question	Answer	Marks
5(b)	1 mark for correct logic gate symbol:  Any **four** from: – similar to an OR gate – It has (at least) two inputs – Output will be high/1 if both inputs are different – Output will be high/1 if either input is high – Output will be low/0 if both inputs are high – Output will be low/0 if both inputs are low	5

Q 15) March 2018 P12 (India)

Question	Answer	Marks
7(a)	4 marks for 8 correct outputs 3 marks for 6 correct outputs 2 marks for 4 correct outputs 1 mark for 2 correct outputs	4

A	B	C	X
0	0	0	**1**
0	0	1	**0**
0	1	0	**1**
0	1	1	**1**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

Question	Answer	Marks
7(b)	1 mark per gate in correct location	6

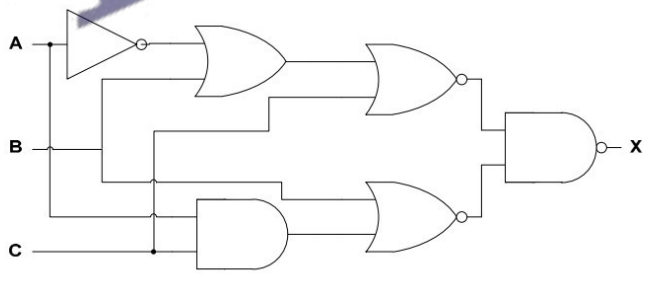


Question	Answer	Marks
7(c)	4 marks for 8 correct outputs 3 marks for 6 correct outputs 2 marks for 4 correct outputs 1 mark for 2 correct outputs	4

A	B	C	X
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**1**
1	0	0	**0**
1	0	1	**0**
1	1	0	**0**
1	1	1	**0**

Q 16) Summer 2018 P11

Question	Answer	Marks
6(a)	1 mark for each correct logic gate (with the correct direction of input(s))	6

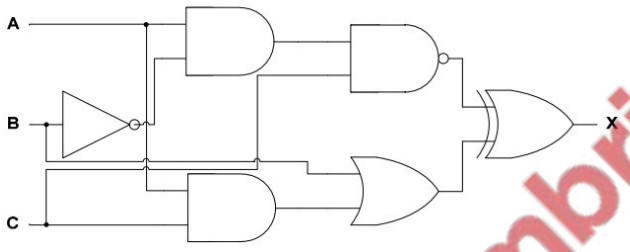


Question	Answer	Marks
6(b)	4 marks for 8 correct outputs 3 marks for 6 or 7 correct outputs 2 marks for 4 or 5 correct outputs 1 mark for 2 or 3 correct outputs	4

A	B	C	Working space	X
0	0	0		**1**
0	0	1		**1**
0	1	0		**1**
0	1	1		**1**
1	0	0		**0**
1	0	1		**1**
1	1	0		**1**
1	1	1		**1**

Q 17) Summer 2018 P12

7(a)	1 mark for each correct logic gate with correct direct of input(s):	6

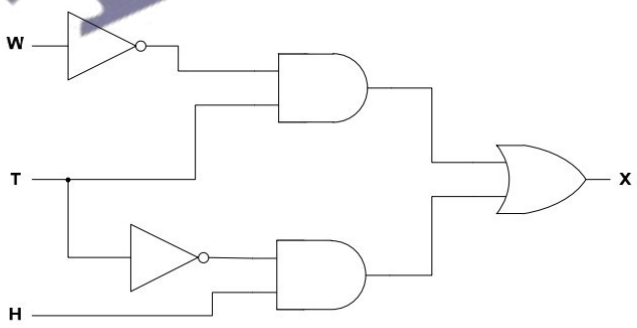


7(b)	4 marks for 8 correct outputs 3 marks for 6 or 7 correct outputs 2 marks for 4 or 5 correct outputs 1 mark for 2 or 3 correct outputs	4

A	B	C	Working space	X
0	0	0		1
0	0	1		1
0	1	0		0
0	1	1		0
1	0	0		1
1	0	1		1
1	1	0		0
1	1	1		0

Q 18) Winter 2018 P12

Question	Answer	Marks
3	1 mark for each correct logic gate, with correct inputs.	5

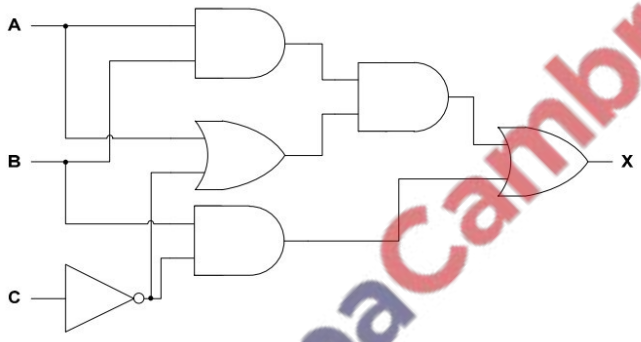


Q 19) Winter 2018 P13

Question	Answer	Marks
10(a)	4 marks for 8 correct outputs 3 marks for 6 or 7 correct outputs 2 marks for 4 or 5 correct outputs 1 mark for 2 or 3 correct outputs	4

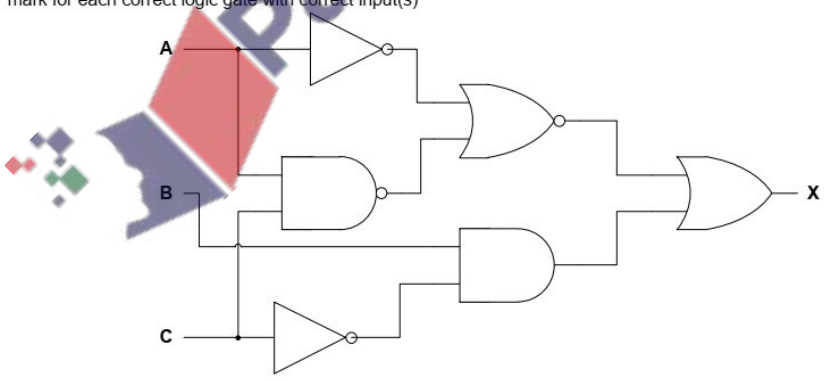
A	B	C	X
0	*0*	*0*	**0**
0	*0*	*1*	**0**
0	*1*	*0*	**1**
0	*1*	*1*	**1**
1	*0*	*0*	**0**
1	*0*	*1*	**1**
1	*1*	*0*	**0**
1	*1*	*1*	**0**

Question	Answer	Marks
10(b)	1 mark per correct gate with correct inputs.	6



Q 20) March 2019 P12

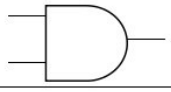
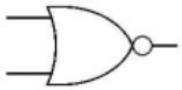
5(a)	1 mark for each correct logic gate with correct input(s)	6



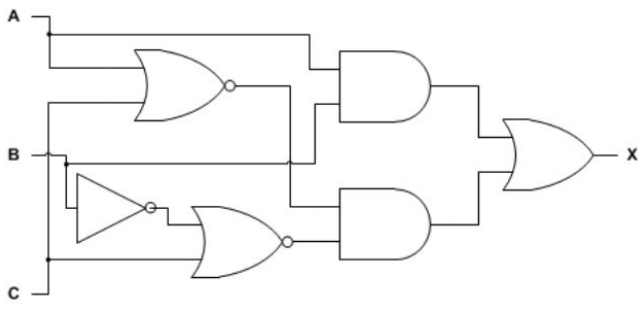
5(b)	4 marks for 8 correct outputs 3 marks for 6/7 correct outputs 2 marks for 4/5 correct outputs 1 mark for 2/3 correct outputs	4

A	B	C	Working space	X
0	0	0		**0**
0	0	1		**0**
0	1	0		**1**
0	1	1		**0**
1	0	0		**0**
1	0	1		**1**
1	1	0		**1**
1	1	1		**1**

Q 21) Summer 2019 P11

2(a)	1 mark for correct name, 1 mark for correct gate symbol – AND 	2
2(b)	1 mark for correct name, 1 mark for correct gate symbol – NOR 	2
2(c)	1 mark for correct name, 1 mark for correct gate symbol – NAND 	2

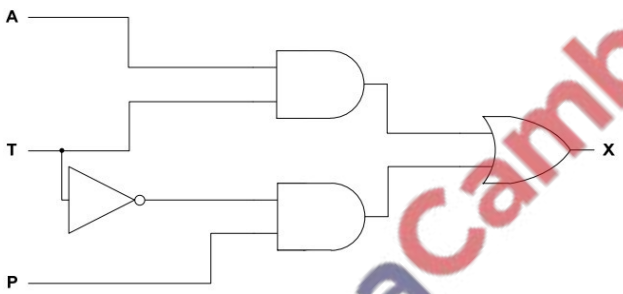
Q 22) Summer 2019 P12

8(a)	1 mark per each correct logic gate, with correct input(s) 	6

8(b)	4 marks for 8 correct outputs 3 marks for 6/7 correct outputs 2 marks for 4/5 correct outputs 1 mark for 2/3 correct outputs	4

A	B	C	Working space	X
0	0	0		**0**
0	0	1		**0**
0	1	0		**1**
0	1	1		**0**
1	0	0		**0**
1	0	1		**0**
1	1	0		**1**
1	1	1		**1**

Q 23) Winter 2019 P13

Question	Answer	Marks
4(a)	**One** mark for each correct logic gate with correct input(s) 	4

2210/13 Cambridge O Level – Mark Scheme **PUBLISHED** October/November 2019

Question	Answer	Marks
4(b)	**Four** mark for 8 correct outputs **Three** marks for 6 or 7 correct outputs **Two** mark for 4 or 5 correct outputs **One** mark for 2 or 3 correct outputs	4

A	T	P	Working space	X
0	0	0		**0**
0	0	1		**1**
0	1	0		**0**
0	1	1		**0**
1	0	0		**0**
1	0	1		**1**
1	1	0		**1**
1	1	1		**1**

4(c)	**Six** from: ∞ Sensor sends a signal/reading/data to the microprocessor ∞ Signal/reading/data is analogue and is converted to digital using ADC ∞ Reading/data is stored in the system ∞ Microprocessor compares data/reading to the pre-set value of 7 ∞ If value is greater than 7 … ∞ … a signal/data is sent by the microprocessor to display a warning message on a monitor ∞ The process is continuous	6

Q 24) Winter 2019 P12

Question	Answer	Marks
8(a)	∞ X = 1 if (A is 1 XOR C is 1) OR (B is 1 NAND C is NOT 1) ∞ X = (A XOR C) OR (B NAND NOTC) **One** mark for each bullet: ∞ (A XOR C) ∞ OR ∞ (B NAND NOTC)	3

Question	Answer	Marks
8(b)	**Four** marks for 8 correct outputs **Three** marks for 6 or 7 correct outputs **Two** marks for 4 or 5 correct outputs **One** mark for 2 or 3 correct outputs	4

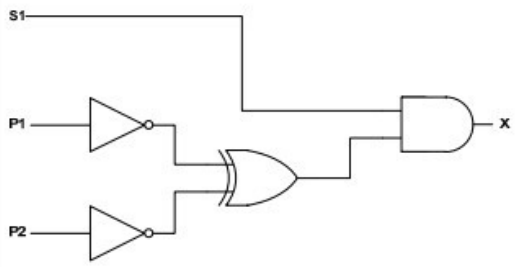
A	B	C	Working space	X
0	0	0		1
0	0	1		1
0	1	0		0
0	1	1		1
1	0	0		1
1	0	1		1
1	1	0		1
1	1	1		1

Q 25) March 20 P12

Question	Answer	Mark
6(a)		4

A	B	C	Working space	X
0	0	0		0
0	0	1		0
0	1	0		0
0	1	1		1
1	0	0		1
1	0	1		1
1	1	0		0
1	1	1		1

4 marks for 8 correct outputs
3 marks for 6/7 correct outputs
2 marks for 4/5 correct outputs
1 mark for 2/3 correct outputs

Question	Answer	Mark
6(b)	1 mark for each correct logic gate:  NOTE: Can also award 4 marks to a circuit that shows X = (P1 XOR P2) AND (S1)	4

Q 26) Summer 20 P12

Question	Answer	Marks
4(a)(i)	– NAND 	2
4(a)(ii)	– NOR 	2

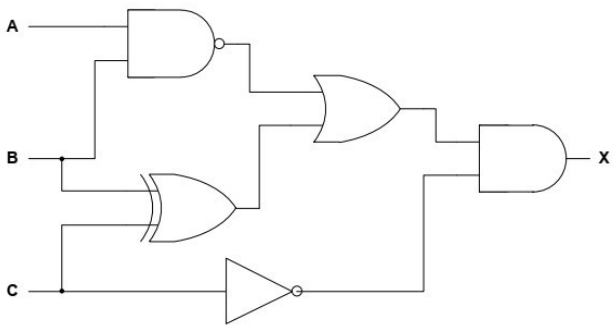
Question	Answer	Marks
4(b)		4

A	B	C	Working space	X
0	0	0		0
0	0	1		0
0	1	0		1
0	1	1		1
1	0	0		0
1	0	1		0
1	1	0		1
1	1	1		1

4 marks for 8 correct outputs
3 marks for 6 or 7 correct outputs
2 marks for 4 or 5 correct outputs
1 mark for 2 or 3 correct outputs

Q 27) 15a Summer 20 P11

2(a)



1 mark for each correct gate.

5

2(b)

A	B	C	Working space	X
0	0	0		1
0	0	1		0
0	1	0		1
0	1	1		0
1	0	0		1
1	0	1		0
1	1	0		1
1	1	1		0

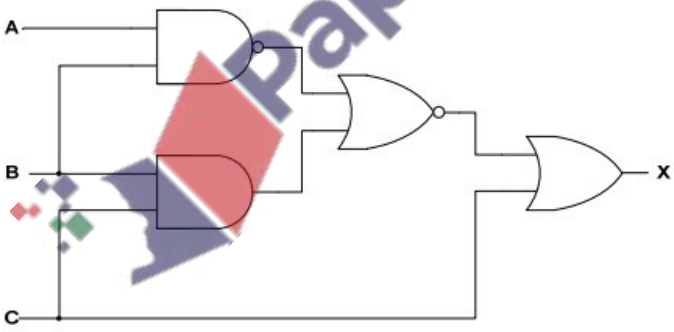
4 marks for 8 correct outputs
3 marks for 6 or 7 correct outputs
2 marks for 4 or 5 correct outputs
1 mark for 2 or 3 correct outputs

4

Q 28) Winter 20 P12

4(a)

One mark for each correct logic gate with correct input:



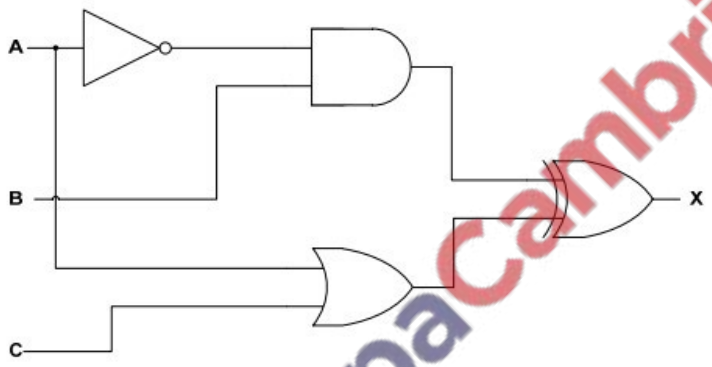
4

4(b)	**Four** marks for 8 correct outputs **Three** marks for 6/7 correct outputs **Two** marks for 4/5 correct outputs **One** mark for 2/3 correct outputs	4

A	B	C	Working space	X
0	0	0		**0**
0	0	1		**1**
0	1	0		**0**
0	1	1		**1**
1	0	0		**0**
1	0	1		**1**
1	1	0		**1**
1	1	1		**1**

Q 29) Winter 20 P13

10(a)	**One** mark for each correct logic gate with the correct input:	4



10(b)	**Four** marks for 8 correct outputs **Three** marks for 6/7 correct outputs **Two** marks for 4/5 correct outputs **One** mark for 2/3 correct outputs	4

A	B	C	Working space	X
0	0	0		**0**
0	0	1		**1**
0	1	0		**1**
0	1	1		**0**
1	0	0		**1**
1	0	1		**1**
1	1	0		**1**
1	1	1		**1**

Q 30) March 20 P12

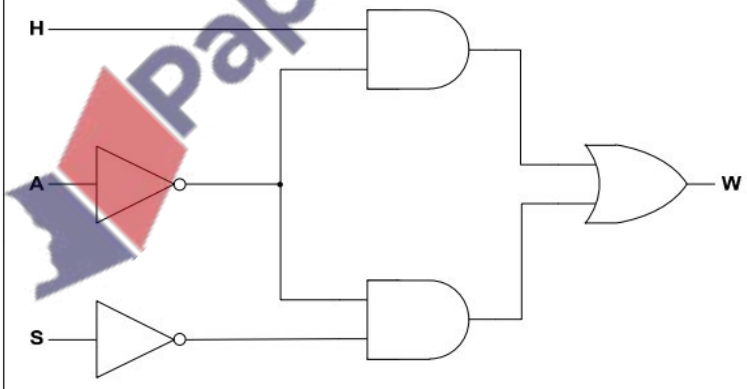
5(a)

Truth table			Logic gate	
A	B	Output	NAND	[1]
0	0	1		
0	1	1		
1	0	1		
1	1	0		
A	B	Output	XOR / Exclusive OR	[1]
0	0	0		
0	1	1		
1	0	1		
1	1	0		
A	B	Output	NOR	[1]
0	0	1		
0	1	0		
1	0	0		
1	1	0		

3

5(b)

One mark for each logic gates with correct inputs



- NOT A
- NOT S
- H AND NOT A
- NOT A AND NOT S
- Final OR

5