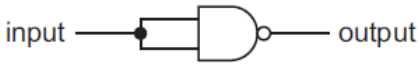
Electronics – 2020 IGCSE 0625

1. March/2020/Paper_22/No.35

The two inputs of a NAND gate are joined together.



Which truth table represents the action of this gate?

A

input	output
0	0
1	0

B

input	output
0	1
1	0

C

input	output
0	0
1	1

D

input	output
0	1
1	1

2. March/2020/Paper_42/No.9

(a) State the name of the logic gate with the symbol shown in Fig. 9.1.

Fig. 9.1

..... [1]

(b) State the name of the logic gate with the truth table shown in Table 9.1.

Table 9.1

input	output
0	1
1	0

..... [1]

(c) Fig. 9.2 shows a digital circuit.

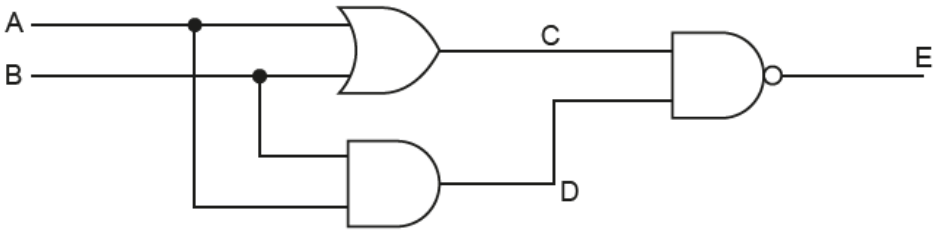


Fig. 9.2

Complete the truth table in Table 9.2 for this circuit for all possible combinations of input.

Table 9.2

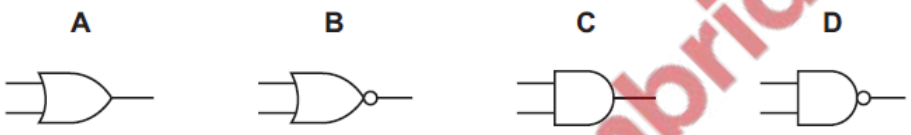
A	B	C	D	E
		1	1	
		1	0	
		1	0	
		0	0	

[4]

[Total: 6]

3. June/2020/Paper_21/No.32

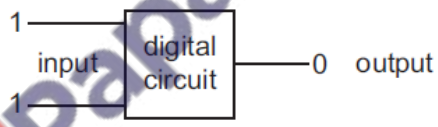
Which symbol represents an OR gate?



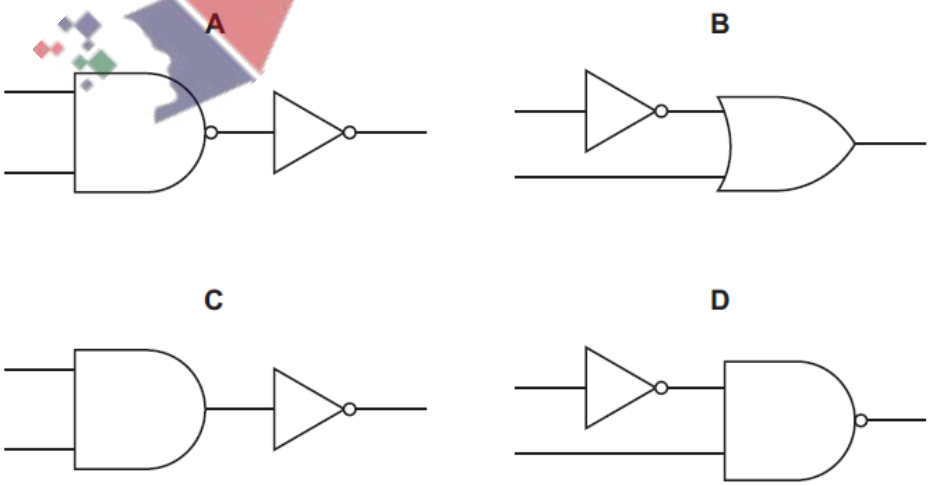
4. June/2020/Paper_21/No.33

A digital circuit consists of two logic gates.

When the input to the circuit is 1 and 1, the output is 0.

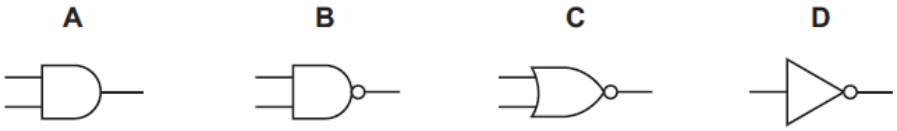


Which combination of logic gates gives this result?



5. June/2020/Paper_22/No.33

Which symbol represents a NAND gate?



6. June/2020/Paper_23/No.33

Which two logic gates each have a high output when both of their inputs are high?

A AND and OR

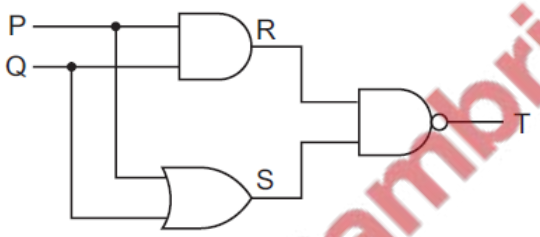
B AND and NOR

C NAND and NOR

D NAND and OR

7. June/2020/Paper_23/No.34

The diagram shows a series of logic gates and part of its corresponding truth table.



P	Q	R	S	T
0	0	0	0	1
0	1			
1	0	0	1	1
1	1	1	1	0

What are the missing values in row 2 of the truth table?

A 0 1 0 **B** 0 1 1 **C** 1 0 0 **D** 1 1 1

8. June/2020/Paper_41/No.9

(a) Describe how a digital signal differs from an analogue signal. You may draw a diagram.

.....

.....

..... [2]

(b) **(i)** In the appropriate box, draw the symbol for an AND gate and the symbol for an OR gate.

AND gate	OR gate

[1]

(ii) State how the behaviour of an AND gate differs from that of an OR gate.

.....

..... [1]

(c) An arrangement of logic gates A, B and C is shown in Fig. 9.1. The arrangement has two inputs, X and Y and two outputs P and Q.

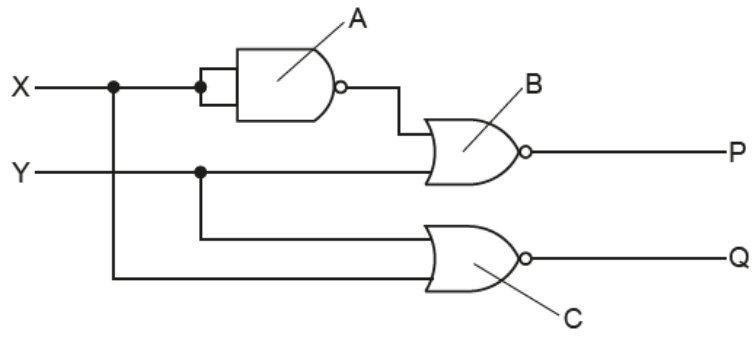


Fig. 9.1

Output P of logic gate B has logic state 1 (high).

(i) Determine the logic states of the two inputs of logic gate B.

upper input = ...

lower input = ...

[1]

(ii) Determine and explain the logic state of output Q.

.....

.....

.....

.....

logic state of Q = ... [3]

[Total: 8]

9. June/2020/Paper_42/No.9

(a) Complete the truth table shown in Table 9.1 for a NAND gate.

Table 9.1

input 1	input 2	output
0	0	
0	1	
1	0	
1	1	

[1]

(b) The circuit shown in Fig. 9.1 contains two different types of gate, labelled X and Y.

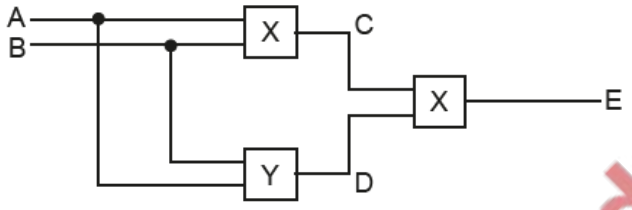


Fig. 9.1

Table 9.2 shows a partially completed truth table for this circuit.

Table 9.2

input		intermediate point		output
A	B	C	D	E
0	0	0	0	
0	1	1	0	
1	0	1	0	
1	1	1	1	

(i) From Table 9.2, deduce the name of logic gate Y.

Ring your answer from the list.

AND NAND NOR NOT OR [1]

(ii) Complete the truth table in Table 9.2. [2]

(c) There is a current of 3.0A in a copper wire. Calculate how many electrons pass through the copper wire every 60 s. The charge on an electron is 1.6×10^{-19} C.

number of electrons = ... [3]

[Total: 7]