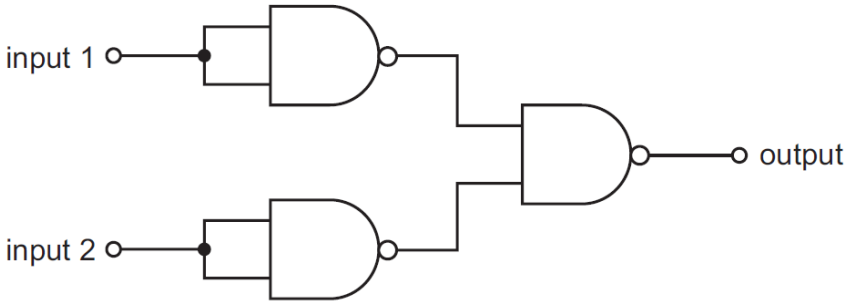
Electronics – 2021 IGCSE 0625

1. June/2021/Paper_21/No.33

Three NAND gates are connected in a single chip as shown.



The whole chip behaves as a single logic gate.

Which type of logic gate does the chip act as?

A AND gate

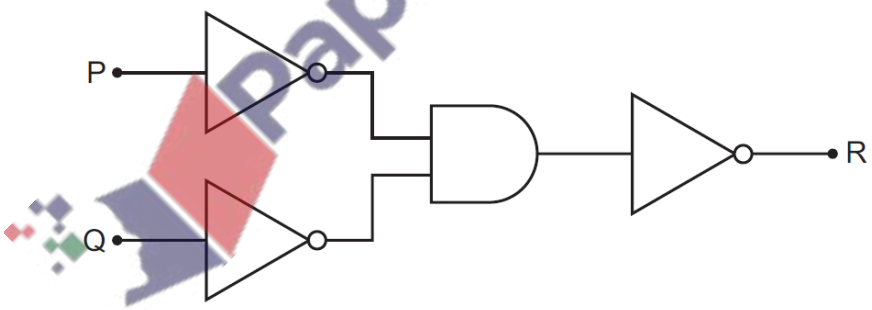
B NAND gate

C NOR gate

D OR gate

2. June/2021/Paper_22/No.34

The diagram shows a combination of four logic gates that produce an output signal at R that depends on the states of the inputs P and Q.



Which single logic gate produces the same effect as the combination?

A AND **B** NAND **C** NOR **D** OR

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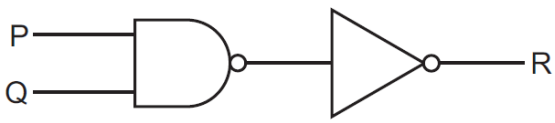
3. June/2021/Paper_23/No.33

Which combination of two gates will result in the truth table shown?

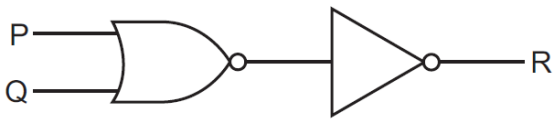
P	Q	R
0	0	0
0	1	1
1	0	1
1	1	1

A

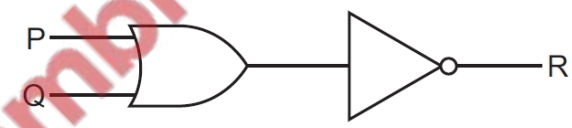


B

C

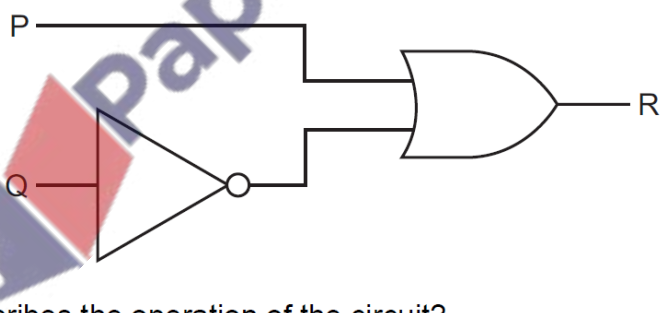


D



4. March/2021/Paper_22/No.35

The circuit shown contains two gates.



Which truth table describes the operation of the circuit?

A

P	Q	R
0	0	0
0	1	1
1	0	1
1	1	1

B

P	Q	R
0	0	0
0	1	0
1	0	1
1	1	1

C

P	Q	R
0	0	1
0	1	0
1	0	0
1	1	0

D

P	Q	R
0	0	1
0	1	0
1	0	1
1	1	1

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5. June/2021/Paper_43/No.8

(a) State the difference between an analogue signal and a digital signal. You may draw a diagram to help explain your answer.

.....

..... [2]

(b) Draw the symbol for a NOR gate.

[1]

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(c) Fig. 8.1 shows a combination of logic gates X, Y and Z. The gates are not represented by the standard symbols.

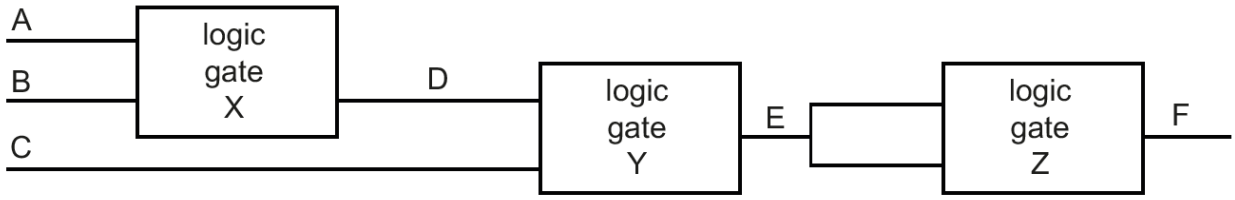

Fig. 8.1

Table 8.1 shows a partly completed truth table for this combination of logic gates.

Table 8.1

inputs			intermediate points		output
A	B	C	D	E	F
0	0	0	0	0	
0	1	0	0	0	
1	0	1	0	1	
1	1	1	1	1	
0	0	0	0	0	
0	1	0	0	0	
1	0	1	0	1	
1	1	1	1	1	

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(i) From Table 8.1, deduce:

1. the name of logic gate X

..... [1]

2. the name of logic gate Y.

..... [1]

(ii) Logic gate Z is a NAND gate.

Complete column F of Table 8.1. [2]

[Total: 7]

6. March/2021/Paper_42/No.9

(a) Write down the truth table for an OR gate.

[2]

(b) Draw the symbol for a NOR gate.

[1]

(c) Fig. 9.1 shows a digital circuit designed to produce the values shown in Table 9.1 for the output S from the two inputs P and Q.

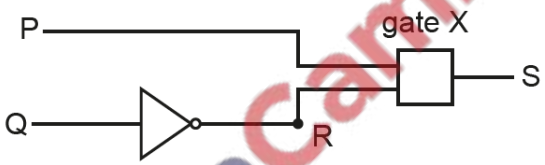

Fig. 9.1

(i) Table 9.1 is the truth table for the circuit shown in Fig. 9.1.

Table 9.1

P	Q	R	S
0	0		0
0	1		0
1	0		1
1	1		0

Complete the column for point R in Table 9.1. [1]

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(ii) State which type of gate is used for gate X. Explain your answer.

statement .....

explanation .....

.....

.....

[3]

[Total: 7]

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