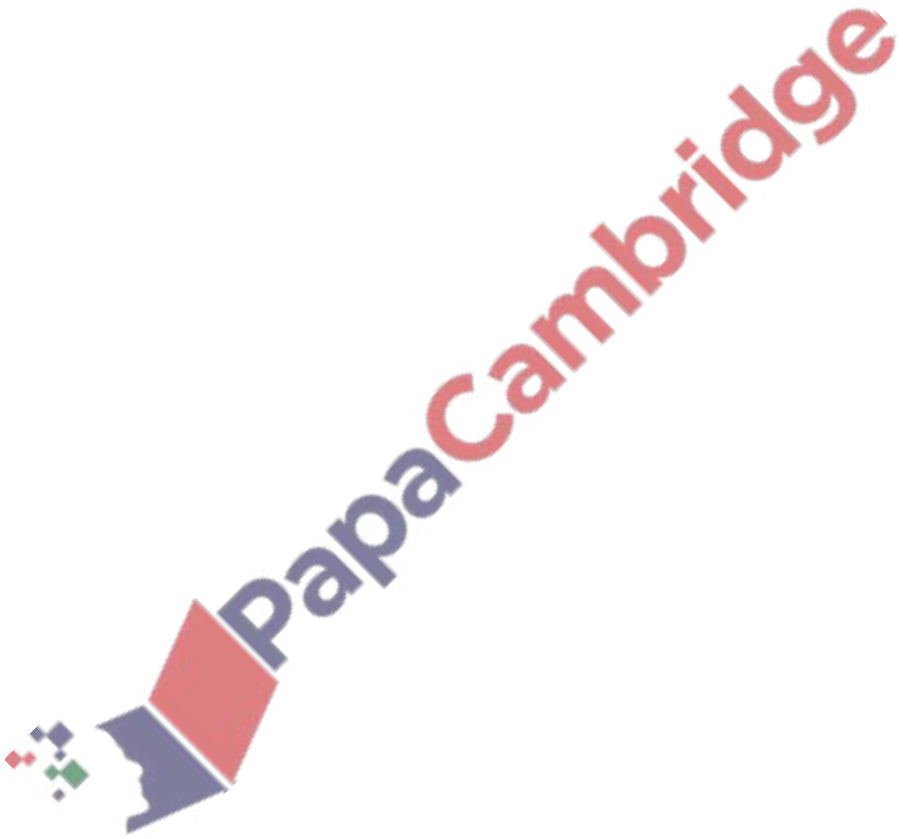
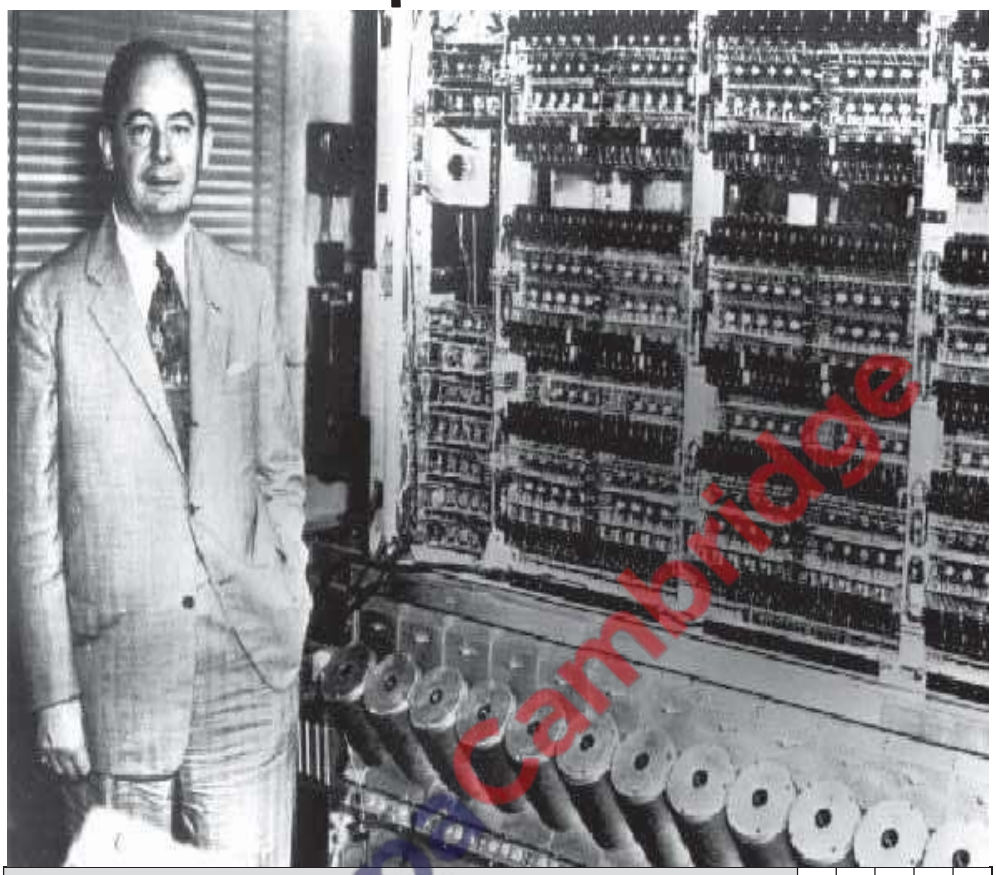
1.3.2

Computer Architecture For O Levels


PapaCambridge

Chapter 4

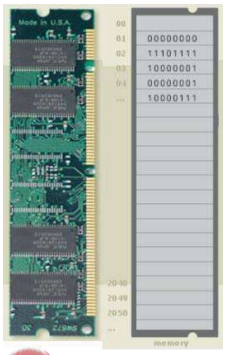
1.3.2 Computer Architecture



Learning Outcome	To Read	Have Read	To Revise	Have Revised	Prepared
1.3.2: Computer architecture and the fetch-execute cycle					
Show understanding of the basic Von Neumann model for a computer system and the stored program concept (program instructions and data are stored in main memory and instructions are fetched and executed one after another)					
Describe the stages of the fetch-execute cycle					

Von Neumann Architecture

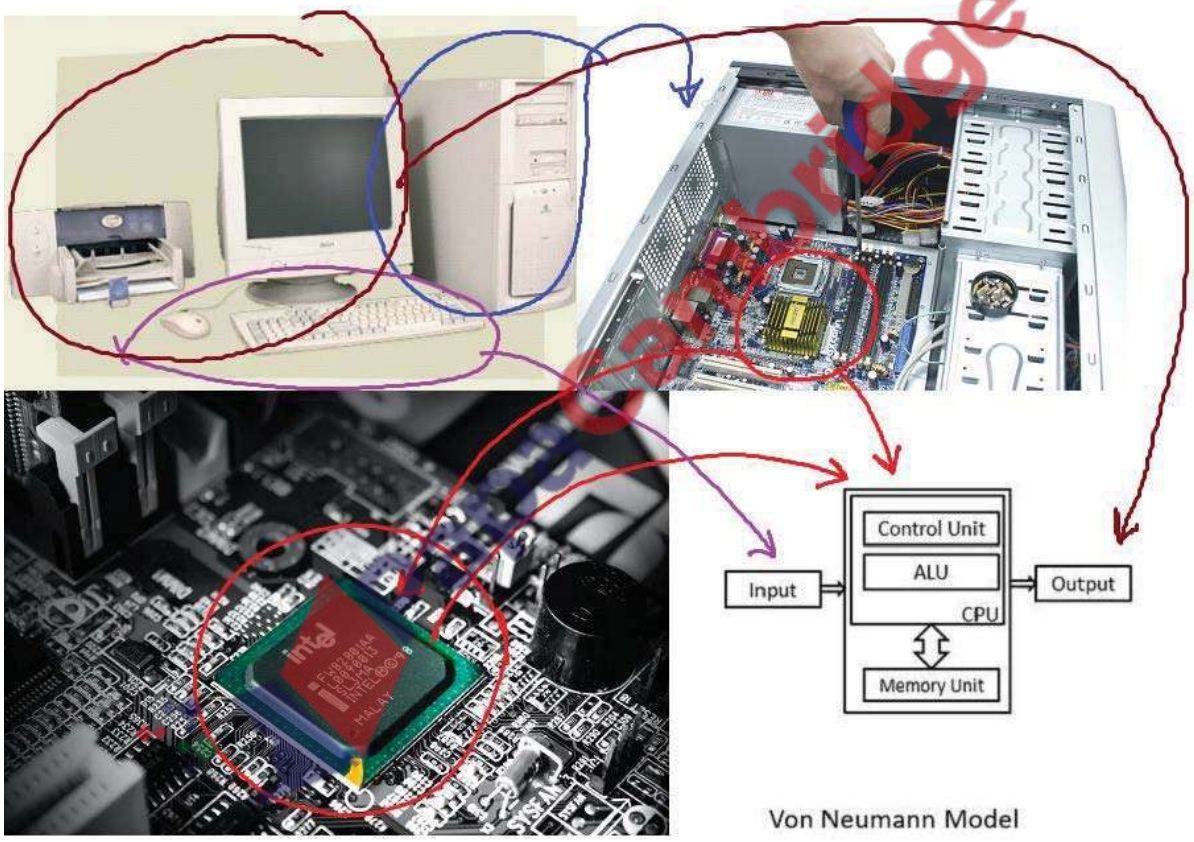
The idea about how computers should be built was proposed by John von Neumann in 1945. Von Neumann gave an idea how to build computer. This idea is also called the **von Neumann Architecture** or **Model**.



A computer should have input/output devices, Arithmetic Logic Unit (ALU), Control Unit (CU) and computer memory (storage device).

Firstly programs should be stored in computer's memory (storage devices). From storage devices programs should be loaded into CPU (ALU & CU) for execution.

This is still the basis for computers today.



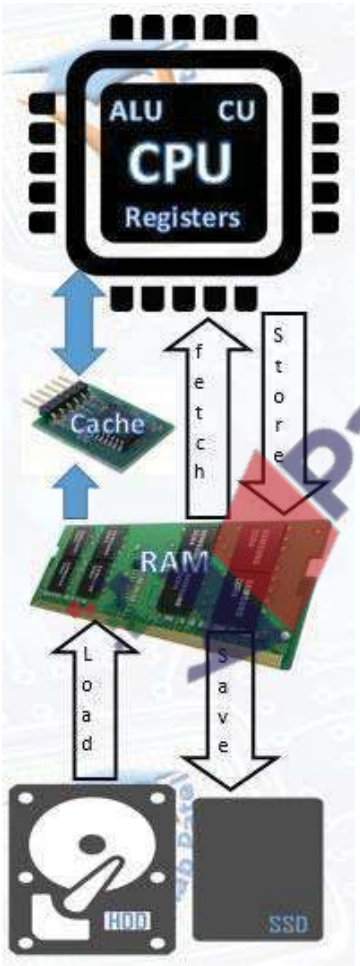
Von Neumann Model

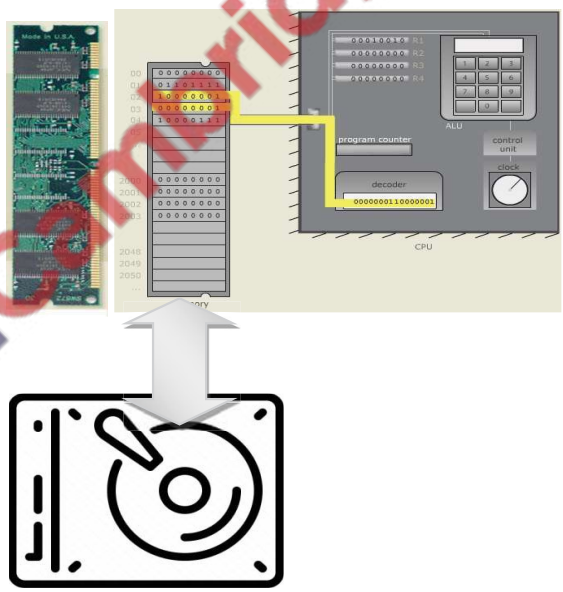
Stored Program Concept:

The idea given by von Neumann, according to this concept computer should have storage device to store data and instruction to be processed. Data and instructions are first stored in secondary storage (HDD or SSD). Then they are loaded in main memory (RAM. Form main memory data and instructions are fetched in registers inside CPU. Decoder of CU decodes the instruction and ALU executes the instructions and results are stored firstly in main memory and then in secondary storage.

Examiner Comments on Question to explain Stored Program Concept

This question appeared to be very challenging for candidates. Many candidates described the fetch execute cycle. It would be helpful if candidates understood that the stored program concept is a specific infrastructure for the central processing unit and not the fetch execute cycle. It would be encouraging to see candidates demonstrate a more confident level of knowledge of the stored program concept.





Components of von Neumann Model

Von Neumann Model has following four components:

1. Input/Output Devices
2. Memory Unit
3. Control Unit
4. Arithmetic Logic Unit

Input/output (I/O) Devices

The Input/output (I/O) components of a computer are hardware devices that are responsible for getting data from the computer to the user or from the user to the computer.

Data going from the user to the computer is called "input." The two main input devices are the mouse and the keyboard.

Output devices are used to transmit data from the computer's memory to the user. The two output devices almost every computer system has are the monitor and the printer.

Memory Unit

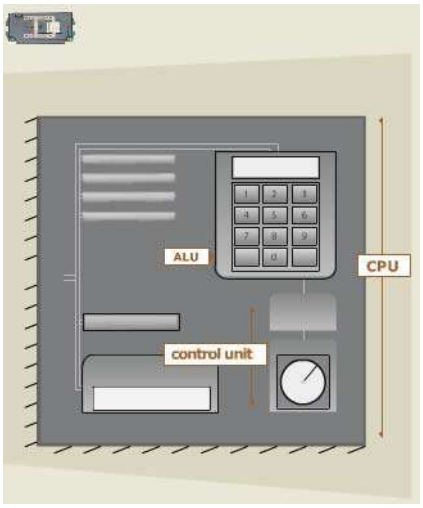
Computer has several types of memory. Memory unit in the Von Neumann model is the main memory, also called RAM or Random Access Memory. It also refers as Immediate Access Store (IAS).

Immediate Access Store (i.e. main memory) holds data and instructions when they are waiting to be processed.

What distinguishes a computer from a calculator is the ability to run a stored program; main memory allows the computer to do that.

RAM can be thought of as a sequence of boxes, called cells, each of which can hold a certain amount of data.

The remaining three components of the von Neumann model of a computer are found inside the Processor.



Control Unit

The control unit controls the sequencing and timing of all operations. It contains a "clock," that is actually a quartz crystal that vibrates million times per second. The clock emits an electronic signal for each vibration. Each separate operation is synchronized to the clock signal. For example 1st pc operates at 4.7 MHz means 4.7 million instructions per second.

The functions of CU are given below:

- Interprets and carries out instruction of program.
- Selects program statements from memory.
- Moves these instructions to instruction registers
- Carries out instructions
- Directs flow of data between components of CPU and to and from other devices.

Arithmetic & Logic Unit (ALU)

Arithmetic unit perform arithmetical operations like +, -, *, and / while logical unit are to compare two quantities. Logical operations are important in computer programming.

ALU can be thought of as being similar to a calculator, except that, in addition to normal math, it can also do logical (true/false) operations.

The functions of ALU are given below:

- The arithmetic unit carries out arithmetic like addition, division.
- The logic unit enables the processor to make comparison like =, <, > and logical decisions like AND, OR, NOT.
- The arithmetic logic unit carries out communication with peripheral devices.
- It also carries out bit shifting operation.

Register:

Registers are located on the CPU, and used temporarily for storing data. Because the registers are close to the ALU, they are made out of fast memory, efficiently speeding up calculations.

Registers store data fetched from Immediate Access Store i.e. main memory.

Immediate Access Store (i.e. main memory) holds data and instructions when they are waiting to be processed.

Register Holds data or instructions temporarily when they are being processed.

There are 16 registers. Some examples are

a) **Program Counter (PC)** - an incrementing counter that keeps track of the **next memory address** of the instruction that is to be executed once the execution of the current instruction is completed.

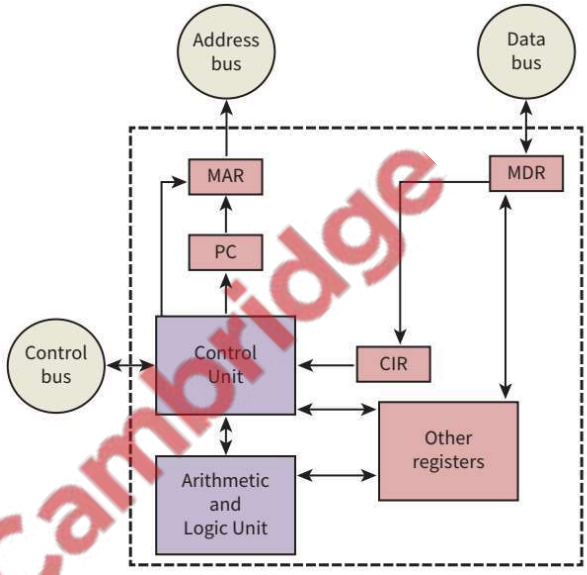
b) **Memory Address Register (MAR)** - the address in main memory that is currently being read or written

c) **Memory Buffer/Data Register (MBR/MBR)** - a two-way register that holds data fetched from memory (and ready for the CPU to process) or data waiting to be stored in memory

d) **Current Instruction register (CIR)** - a temporary holding ground for the instruction that has just been fetched from memory

e) **Accumulator Register (ACC)** is used for storing data for ALU to process and the results those are produced by the ALU.

Buses: "The set of wires used to travel signals to and from CPU and different components of computer is called Bus."



Bus is a group of parallel wires that is used as a communication path. As a wire transmits a single bit so 8-bits bus can transfer 8 bits (1 byte) at a time and 16-bits bus can transfer 16 bits (2 bytes) and so on. There are three types of buses according to three types of signals, these are:

a) **Data Bus:** "The buses which are used to transmit data between CPU, memory and peripherals are called Data Bus."

b) **Address Bus:** "The buses which are connecting the CPU with main memory and used to identify particular locations (address) in main memory where data is stored are called Address Buses."

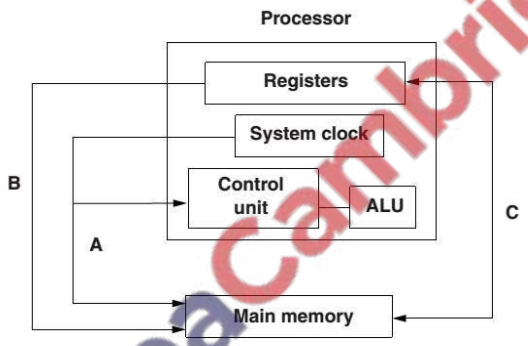
c) **Control Bus:** The wires which are used to transmit the control signals (instructions) generated by Control Unit to the relevant component of the computer.

Example Question

Q 4.1 (a) One of the key features of von Neumann computer architecture is the use of buses. Three buses and three descriptions are shown below. Draw a line to connect each bus to its correct description.

Address bus	This bus carries signals used to coordinate the computer's activities
Control bus	This bi-directional bus is used to exchange data between processor, memory and input/ output devices
Data bus	This uni-directional bus carries signals relating to memory addresses between processor and memory

Q 4.2)



The diagram above shows a simplified form of processor architecture.

Name the three buses labelled A, B and C.

A .....

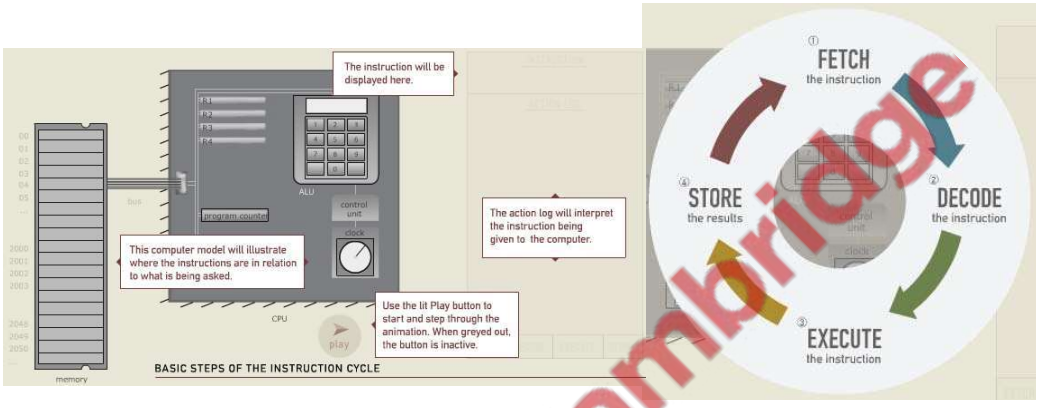
B .....

C ..... [3]

Fetch-Execute Cycle:

At its core, all the computer ever does is, execute one instruction in memory after another, over and over. Although there are many different possible (assembly language) instructions that the computer can execute, the basic steps involved in executing an instruction are always the same, and they are called the instruction cycle.

1. **Fetch** the instruction (transfer the instruction from main memory to the decoder)
2. **Decode** the instruction (from machine language)
3. **Execute** the instruction (e.g., add, divide, load, store...)
4. **Store** the result (for instructions like ADD, place the 'answer' in the specified register.)



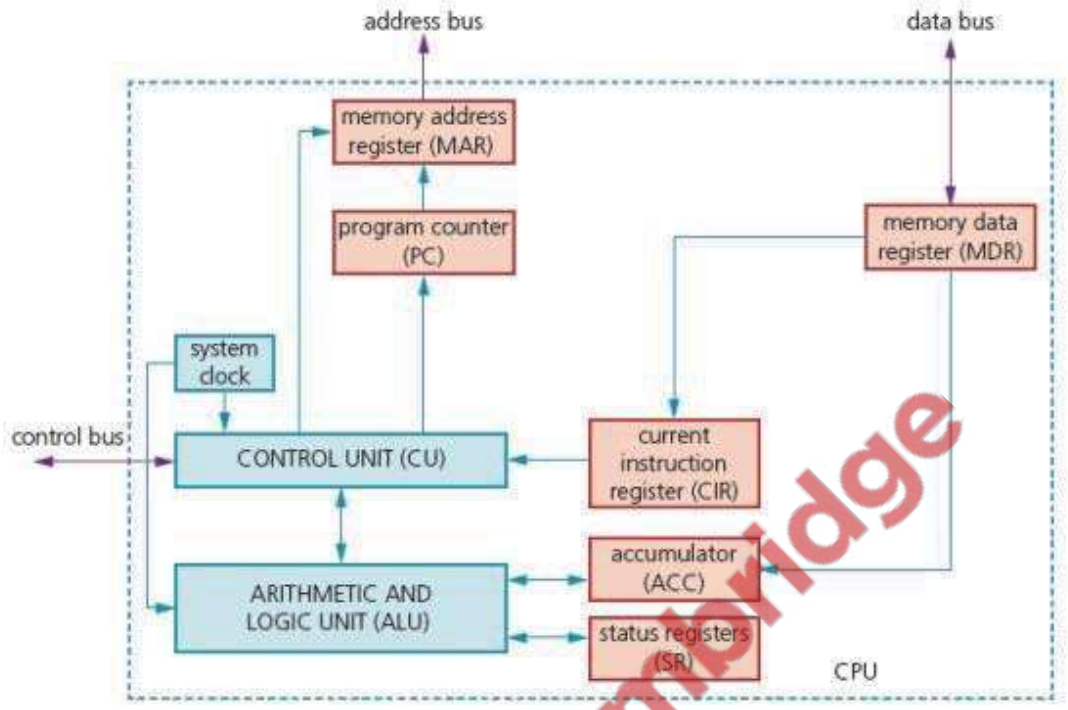
The control unit guides the computer's components through this cycle to execute one instruction. When that instruction is done, the cycle starts all over again with the next instruction.

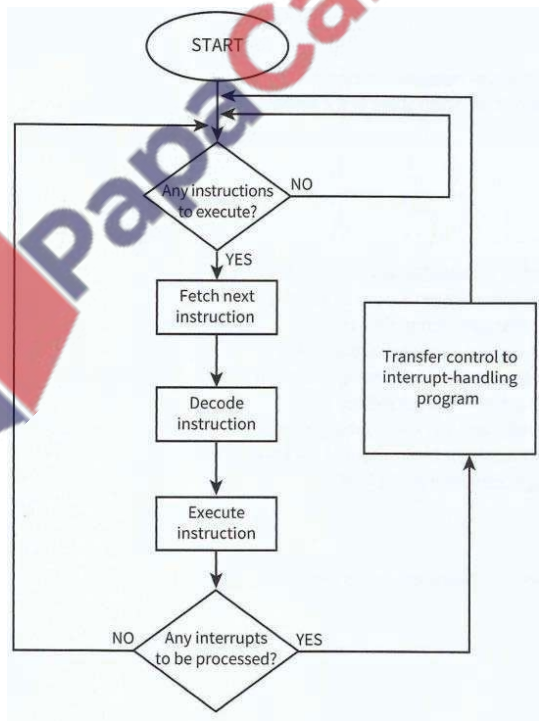
Registers/circuits involved

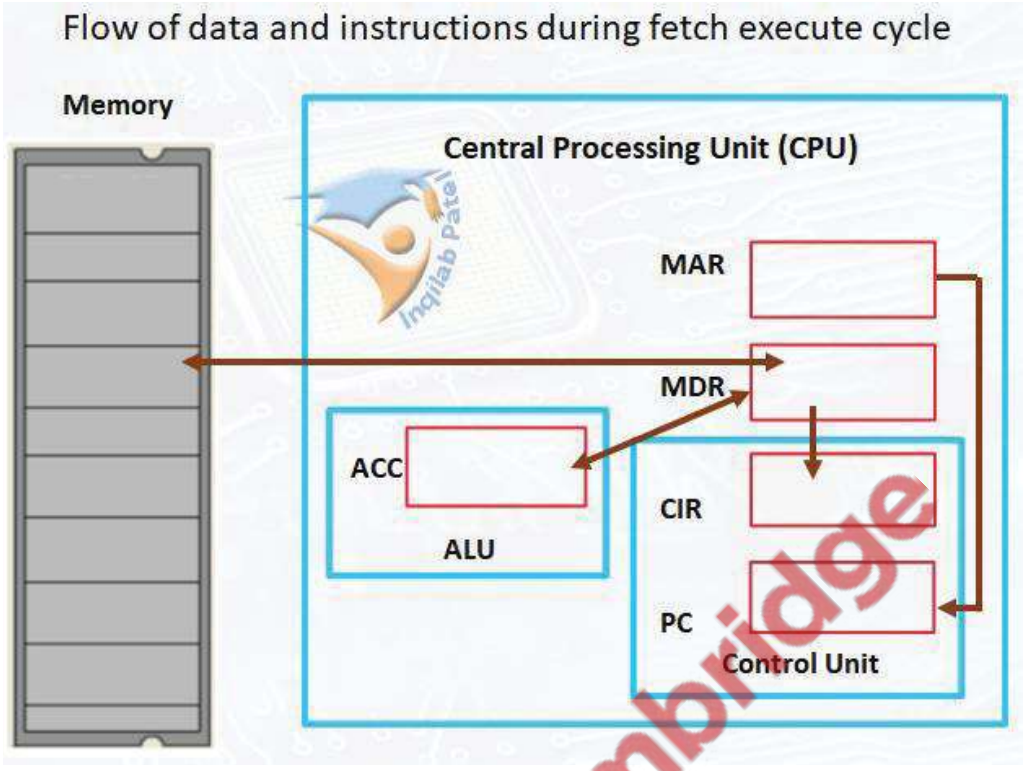
The circuits used in the CPU during the cycle are:

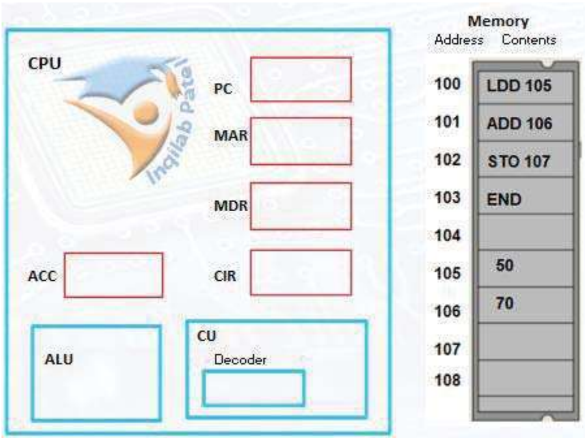
- **Program Counter (PC)** - an incrementing counter that keeps track of the **next memory address** of the instruction that is to be executed once the execution of the current instruction is completed.
- **Memory Address Register (MAR)** - the address in main memory that is currently being read or written
- **Memory Buffer Register (MBR)** - a two-way register that holds data fetched from memory (and ready for the CPU to process) or data waiting to be stored in memory
- **Current Instruction register (CIR)** - a temporary holding ground for the instruction that has just been fetched from memory
- **Accumulator Register (ACC)** is used for storing data for ALU to process and the results those are produced by the ALU.
- **Control Unit (CU)** - decodes the program instruction in the CIR, selecting machine resources such as a data source register and a particular arithmetic operation, and coordinates activation of those resources

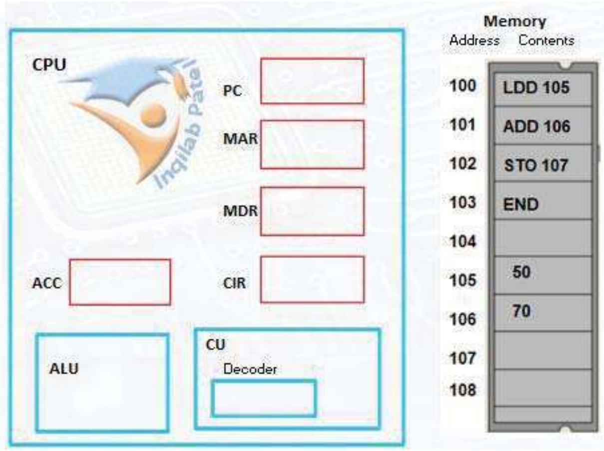
- **<u>Arithmetic logic unit</u> (ALU)** - performs mathematical and logical operations

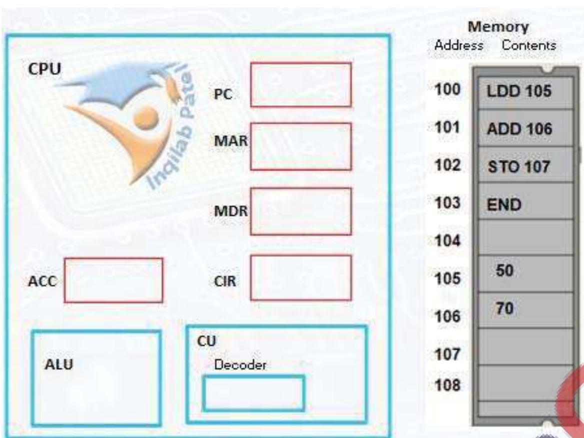


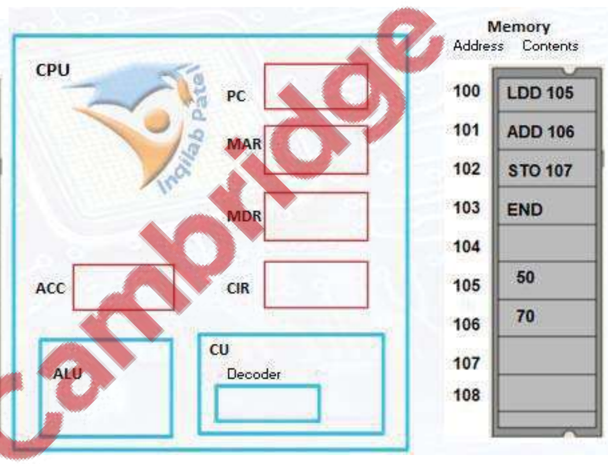


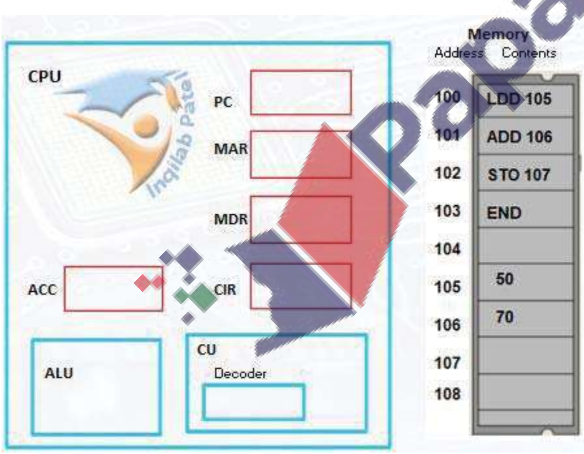


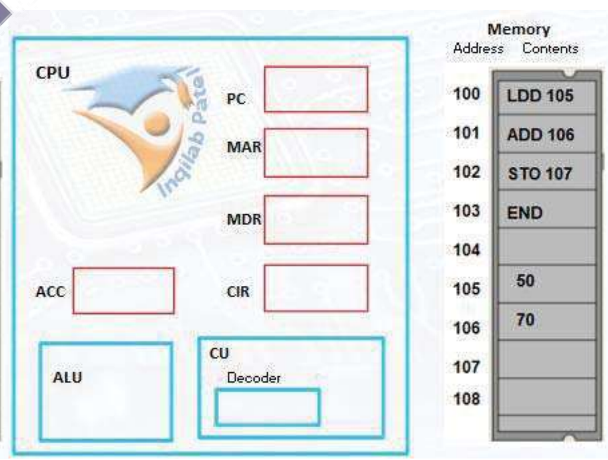

CPU
PC
MAR
MDR
ACC
CIR
ALU
CU
Decoder
Memory
Address Contents
100 LDD 105
101 ADD 106
102 STO 107
103 END
104
105 50
106 70
107
108


CPU
PC
MAR
MDR
ACC
CIR
ALU
CU
Decoder
Memory
Address Contents
100 LDD 105
101 ADD 106
102 STO 107
103 END
104
105 50
106 70
107
108


CPU
PC
MAR
MDR
ACC
CIR
ALU
CU
Decoder
Memory
Address Contents
100 LDD 105
101 ADD 106
102 STO 107
103 END
104
105 50
106 70
107
108


CPU
PC
MAR
MDR
ACC
CIR
ALU
CU
Decoder
Memory
Address Contents
100 LDD 105
101 ADD 106
102 STO 107
103 END
104
105 50
106 70
107
108


CPU
PC
MAR
MDR
ACC
CIR
ALU
CU
Decoder
Memory
Address Contents
100 LDD 105
101 ADD 106
102 STO 107
103 END
104
105 50
106 70
107
108


CPU
PC
MAR
MDR
ACC
CIR
ALU
CU
Decoder
Memory
Address Contents
100 LDD 105
101 ADD 106
102 STO 107
103 END
104
105 50
106 70
107
108

Fill in the following table

Description	PC	MAR	MDR	CIR	Decoder	ACC	ALU

Test Yourself The table shows six stages in the von Neumann fetch-execute cycle.

Put the stages into the correct sequence by writing the numbers 1 to 6 in the right hand column.[6]

Description of stage	**Sequence No**
the instruction is copied from the Memory Data Register (MDR) and placed in the Current Instruction Register (CIR)	
the instruction is executed	
the instruction is decoded	
the address contained in the Program Counter (PC) is copied to the Memory Address Register (MAR)	
the value in the Program Counter (PC) is incremented so that it points to the next instruction to be fetched	
the instruction is copied from the memory location contained in the Memory Address Register (MAR) and is placed in the Memory Data Register (MDR)	

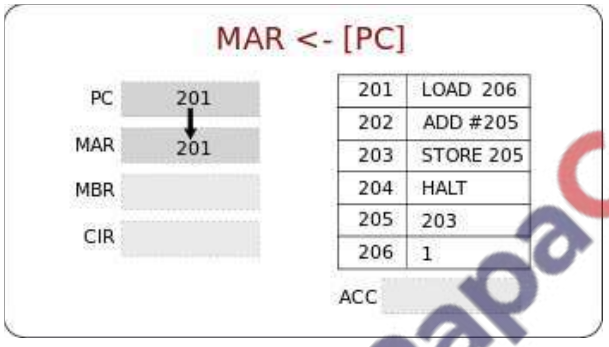
Register Transfer Notation

To describe the cycle we can use register notation. This is a very simple way of noting all the steps involved. In all cases brackets e.g. [PC], means that the contents of the thing inside the brackets are loaded. In the case of the first line, the contents of the program counter are loaded into the Memory Address Register.

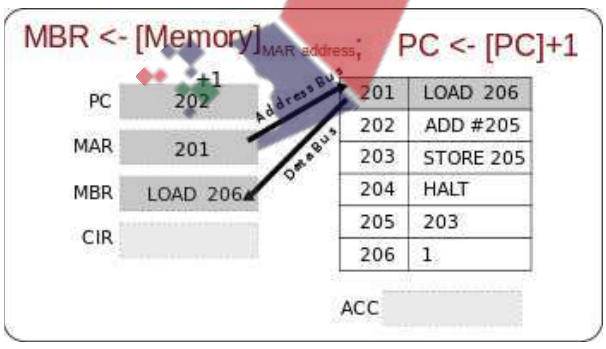
MAR ← [PC]
MBR ← [Memory] ; PC← [PC] +1 (Increment the PC for next cycle at the same time)
CIR ← [MBR]
CIR sends instruction to Decoder of control unit
Decoder decodes
Or ACC← [MBR]
ACC sends data to ALU
ALU executes

Detailed description of Fetch-Decode-Execute Cycle

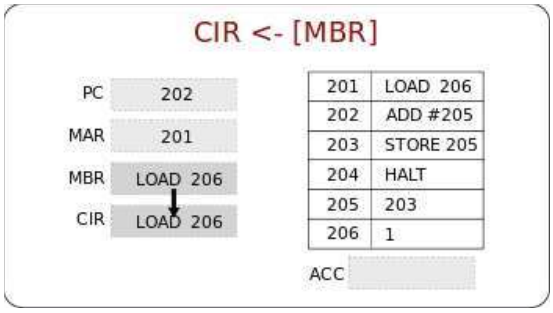
To better understand what is going on at each stage we'll now look at a detailed description:



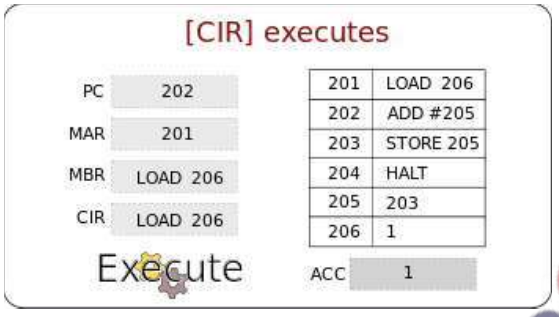
The contents of the Program Counter, the address of the next instruction to be executed, is placed into the Memory Address Register



The address is sent from the MAR along the address bus to the Main Memory. The instruction at that address is found and returned along the data bus to the Memory Buffer Register. At the same time the contents of the Program Counter is increased by 1, to reference the next instruction to be executed.



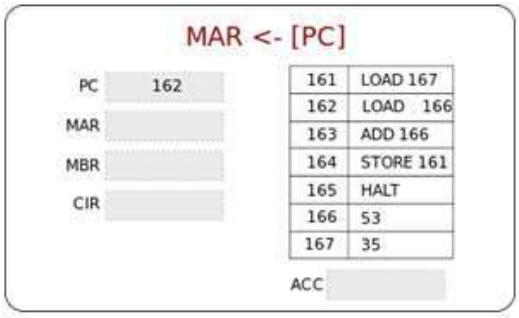
The MBR loads the Current Instruction Register with the instruction to be decoded by decoder of control unit or the MBR loads Accumulator with the data to be executed.

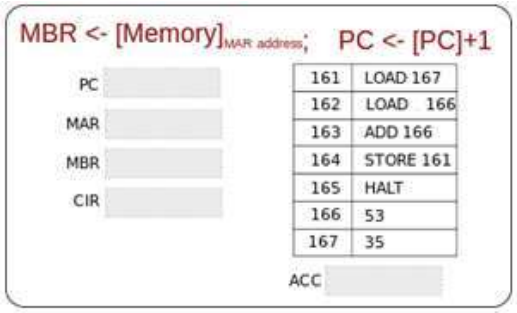


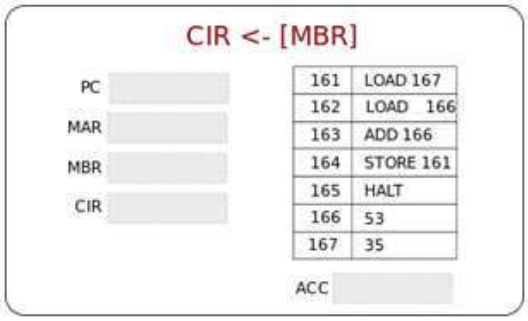
The instruction is decoded and executed using the ALU if necessary.

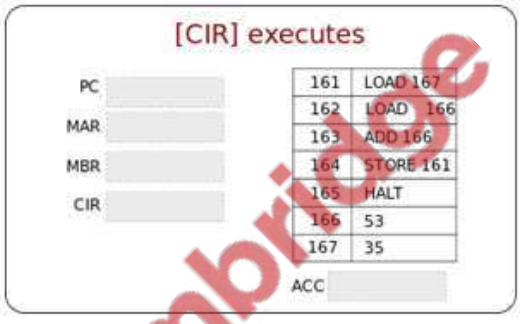
The Cycle starts again!

Q 4.4a) Complete the following diagrams showing each step of the fetch decode execute cycle:









b) The fetch-execute cycle is shown in register transfer notation.

01 MAR ←[PC]

02 PC ←[PC] - 1

03 MDR ←[MAR]

04 CIR ←[MAR]

(a) There are **three** errors in the fetch-execute cycle shown.

Identify the line number of each error and give the correction.

Line number .....

Correction .....

Line number .....

Correction .....

Line number .....

Correction ..... [3]

c) Solve the program shown below:

Address	Contents
1	1010 LDA 1111
10	1111 ADD 1110
11	0000 SUB 1101
100	1111 ADD 1100
101	1111 ADD 1011
110	0000 SUB #5
111	1111 ADD #90
1000	0111 STO 1010
1001	1100 STP
1010	
1011	55
1100	10
1101	5
1110	50
1111	150

Keys:

1010	LDA
1111	ADD
0	SUB
111	STO
1100	STP

Instruction No	PC	MAR	MDR	CIR	ACC	ALU	1010

Practice Questions

Q 4.5) Describe what differs a computer with a calculator

.....

..... **[1]**

Q 4.6) Differentiate an ALU with a calculator.

.....

..... **[1]**

Q 4.7) Von Neumann gave the idea how computer should be built.

a) Describe the purpose of each of the following parts of a processor:

(i) Control unit

.....

..... **[1]**

(ii) Arithmetic & Logic unit

.....

..... **[1]**

(iii) Register

.....

..... **[1]**

b) Draw and label the diagram of von Neumann architecture.

Q 4.8) Draw the diagram and describe the stages of fetch-execute cycle.

Q 4.9) Description of fetch-execute cycle:

.....

.....

.....

..... **[6]**

Q 4.10) The sequence of operations shows, in register transfer notation, the fetch stage of the fetch-execute cycle.

1 MAR←[PC]

2 PC ←[PC] + 1

3 MDR ←[[MAR]]

4 CIR ←[MDR]

• [register] denotes contents of the specified register or memory location

• step 1 above is read as “the contents of the Program Counter are copied to the Memory Address Register”

(i) Describe what is happening at step 2.

.....

..... **[1]**

(ii) Describe what is happening at step 3.

.....

..... **[1]**

(iii) Describe what is happening at step 4.

.....

..... **[1]**

Q 4.11) (a) Describe basic Von Neumann processor architecture.

.....

.....

.....

..... **[3]**

(b) At a particular point in a program, the program counter (PC) contains the value 200.

(i) State the expected value contained in the PC after the instruction held at location 200 has been fetched .....

Explain your answer.

.....

..... **[1]**

Q 4.12) One of the buses found in a typical microprocessor architecture is the control bus. Describe its purpose.

.....

..... **[1]**

Q 4.13) (i) One of the buses found in a typical microprocessor architecture is the control bus. Describe its purpose.

.....

..... **[1]**

Give **one** example of a control signal used.

..... **[1]**

(ii) Name and describe **two** other buses used in a typical microprocessor architecture.

1 .....

2 ..... [2]

Q 4.14) (ii) The contents of some special-purpose registers change as the program is executed. Complete the trace table for the fetching of the **first program instruction (867A)**:

• Show how the contents of the registers change.

• Put a tick in the address bus and/or data bus column to show when there is a signal change on each bus. [5]

Fetch stage	Special purpose registers (Contents shown in hex)				Buses	
	PC	MAR	MDR	CIR	Address bus	Data bus
	58					
MAR ← [PC]						
PC ← [PC] + 1						
MDR ←[[MAR]]						
CIR ← [MDR]						

Q 4.17) The following text includes a description of four stages of the fetch-execute cycle. Use the terms below to complete the text:

Memory Data Register (MDR), Memory Address Register (MAR), Program Counter (PC), Current Instruction Register(CIR), address, data bus, main memory, address bus.

The program instructions are stored in a continuous block of ..... .

The Program Counter stores the ..... of the next instruction to be fetched.

Stage 1: The contents of the Program Counter are copied to

the ..... .Stage 2 The contents of the ..... are then incremented. Stage 3 The value in the Memory Address Register is loaded to

the..... .The data value found at this address is loaded on to

the..... and copied to the ..... .Stage 4 The contents of the Memory Data Register are copied to the..... and. The instruction can now be decoded and executed. [6]

Summer 2019 P12

3 Vanessa writes a paragraph as an answer to an examination question about the central processing unit (CPU).

Use the list given to complete Vanessa's answer by inserting the correct **six** missing terms.

Not all terms will be used.

• Components	• Data	• Decoded
• Executed	• Fetched	• Instructions
• RAM	• ROM	• Secondary storage

The CPU processes ..... and ..... .

An instruction is ..... from ..... into the CPU where it is then ..... . Once this has taken place the instruction is then ..... . [6]

Candidate Example response

Question 3

Example Candidate Response – high	Examiner Comments
3 Vanessa writes a paragraph as an answer to an examination question about the central processing unit (CPU). Use the list given to complete Vanessa's answer by inserting the correct **six** missing terms. Not all terms will be used. • Components • Data • Decoded • Executed • Fetched • Instructions • RAM • ROM • Secondary storage The CPU processes ..data.. and ..instructions.. An instruction is ..fetched.. from ..RAM.. into the CPU where it is then ..decoded.. . Once this has taken place the instruction is then ..executed.. 1 [6]	1 The candidate provides six correct terms, in the correct places. **Total mark awarded = 6 out of 6**

How the candidate could have improved their answer

The candidate provided a fully correct answer that could not have been improved.

Example Candidate Response – middle	Examiner Comments
3 Vanessa writes a paragraph as an answer to an examination question about the central processing unit (CPU). Use the list given to complete Vanessa's answer by inserting the correct **six** missing terms. Not all terms will be used. • Components • Data • Decoded • Executed • Fetched • Instructions • RAM • ROM • Secondary storage The CPU processes ..instructions.. and ..data.. An instruction is ..fetched.. from ..RAM, secondary storage.. 1 into the CPU where it is then ..decoded.. . Once this has taken place the instruction is then ..executed.. [6]	1 The candidate provides an incorrect type of storage that is accessed by the CPU. The CPU cannot access secondary storage to fetch instructions and data. The candidate may misunderstand, as the secondary storage will be where the data is originally stored. **Total mark awarded = 5 out of 6**

How the candidate could have improved their answer

The candidate demonstrated a good understanding of the central processing unit. However, it would have been beneficial if they had understood that the CPU would fetch instructions and data from the RAM and not secondary storage.

Example Candidate Response – low	Examiner Comments
3 Vanessa writes a paragraph as an answer to an examination question about the central processing unit (CPU). Use the list given to complete Vanessa's answer by inserting the correct **six** missing terms. Not all terms will be used. • Components • Data • Decoded • Executed • Fetched • Instructions • RAM • ROM • Secondary storage The CPU processes RAM and Ram 1. An instruction is Fetched from Secondary Storage 2 into the CPU where it is then Decoded. Once this has taken place the instruction is then Executed. [6]	1 The candidate shows misunderstanding of what the CPU processes. They provide two components from the computer, rather than items such as data and instructions. 2 The candidate also misunderstands that the CPU is able to fetch data from secondary storage. It would be beneficial for the candidate to understand that the CPU can only access the RAM. **Total mark awarded = 3 out of 6**

How the candidate could have improved their answer

The candidate misunderstood the CPU although they understood that it had a cycle that fetched, decoded and executed. They misunderstood what the CPU processed. They also showed the same misunderstanding that the CPU fetched data from secondary storage.

Common mistakes candidates made in this question

Some candidates misunderstood that the CPU fetched data and instructions from secondary storage. They may have thought this, as the data may originally have been stored in the secondary storage, however, it would have been beneficial for candidates to have understood that the data needed to be brought into RAM, before it could be accessed by the CPU.

Question 5 (a)

Describe the purpose of each of the following parts of a processor:

(i) Control unit **(ii)** Memory unit **(iii)** ALU

Mark scheme

(i) – Manages the execution of instructions – Fetches each instruction in turn
– Decodes and synchronises its execution...
– by sending control signals to other parts of processor [2]
(ii)– Stores program in current use – Stores data in current use
– Stores parts of OS in current use [2]
(iii)– Carries out arithmetic operations – Carries out comparisons
– Acts as gateway in and out of processor (1 per –, max 2 per dotty, max 6) [2]

Example candidate response – grade A

(i) Control unit

Control unit is that part of processor that instructs all the other components, what to do. There it fetches instructions from the main memory and decodes them, & and then it carry those the execution of those instructions [2]
by the other components. It choreographs the controlling with a clock through

(ii) Memory unit

Memory unit stores instructions and data that are being executed by the processor. If the processor, needs to access this data again, it can access it them quickly from the main memory [2]

(iii) ALU

ALU (Arithmetic logic unit) contains circuitary to manipulate data. It can perform logical and arithmetic operations on data. Furthermore, all input and output device must pass through the ALU. [2]

Examiner comment

In part **(i)**, the answer went way beyond what was necessary for full marks. They referred to the *fetch cycle, execution of decoded instructions, reference to clock* etc. More than enough for full marks. In part**(ii)**, the candidate clearly understood that data and instructions (currently in use) are stored in the memory unit. This reference to *currently in use* distinguished grade A candidates from the grade C candidates, as seen in the example below. The third part was also clearly laid out – *the ALU performs logical and arithmetic operations* is very clear and unambiguous. Lower ability candidates tend to refer to *doing some arithmetic* and *making logical decisions* which indicates a lack of understanding of how the ALU works.

Example candidate response – grade C

(i) Control unit

All computers follow instructions that are given to it in a programe. These instructions are in a particular order in the program and following them and carrying them out. This is the job of a control unit. [2]

(ii) Memory unit

The second part of the processor is where everything that the processor is going to use is stored. This includes all the programme instructions and all the data needed to carry out those instructions. [2]

(iii) ALU

The first task of the ALU is its ability to add numbers with the help of circuitry. The second task is its ability to make logical decisions. The third task is to act like a gat gateway between the processor and parts of the computer. [2]

Examiner comment

Part **(i)** was not really describing the control unit. Part **(ii)** did not mention that data and instructions currently in use are stored here. The third part was sketchy with the candidate describing the ALU as 'adding numbers' and 'making logical decisions'. The only part which was awarded a mark was the reference to the ALU acting as a *gateway.* Candidates at grade C tended to know the terms but were unclear of how it all interlinked and produced very vague, often incorrect, answers to questions of this type.

Example candidate response – grade E

(i) Control unit

It manages the processing.
It fetches the things done in ~~processing~~ Processor

[2]

(ii) Memory unit

It stores ~~what~~ the things ~~in the~~ while processing.
It stores in its memory so it could be used next time.

[2]

(iii) ALU

Arthimatics are done in the ALU.
All the calculations are done in the ALU.

[2]

Examiner comment

The occasional correct word like *fetch* was used, but the candidate had no real understanding of how the control unit works. Part **(ii)** was a little better, with the candidate showing some idea of how the memory unit works but falls short of making some key comments which could gain marks. In part **(iii)**, a reference to arithmetic and calculations was the level of understanding. There was no mention of arithmetic operations or logical comparisons in their answer.

(c) The table shows six stages in the von Neumann fetch-execute cycle.

Put the stages into the correct sequence by writing the numbers 1 to 6 in the right hand column.

Description of stage	Sequence number
the instruction is copied from the Memory Data Register (MDR) and placed in the Current Instruction Register (CIR)	
the instruction is executed	
the instruction is decoded	
the address contained in the Program Counter (PC) is copied to the Memory Address Register (MAR)	
the value in the Program Counter (PC) is incremented so that it points to the next instruction to be fetched	
the instruction is copied from the memory location contained in the Memory Address Register (MAR) and is placed in the Memory Data Register (MDR)	

[6]

Example Candidate Response High, Middle and Low

Description of stage	Sequence number
the instruction is copied from the Memory Data Register (MDR) and placed in the Current Instruction Register (CIR)	4
the instruction is executed	6
the instruction is decoded	5
the address contained in the Program Counter (PC) is copied to the Memory Address Register (MAR)	1
the value in the Program Counter (PC) is incremented so that it points to the next instruction to be fetched.	2
the instruction is copied from the memory location contained in the Memory Address Register (MAR) and is placed in the Memory Data Register (MDR)	3

[6]

Examiner comment – high

In part (c), in common with the vast majority of candidates, this candidate has correctly identified the sequence of stages of the von Neumann fetch-execute cycle.
Marks awarded in part (c) = 6/6

Topical Questions from Past Papers

Q 1) Summer 2015 P11

7 (a) One of the key features of von Neumann computer architecture is the use of buses.
Three buses and three descriptions are shown below.
Draw a line to connect each bus to its correct description.

Address bus	This bus carries signals used to coordinate the computer's activities
Control bus	This bi-directional bus is used to exchange data between processor, memory and input/ output devices
Data bus	This uni-directional bus carries signals relating to memory addresses between processor and memory

(b) The seven stages in a von Neumann fetch-execute cycle are shown in the table below. Put each stage in the correct sequence by writing the numbers 1 to 7 in the right hand column. The first one has been done for you.

Stage	Sequence number
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register)	
the instruction is finally decoded and is then executed	
the PC (program counter) contains the address of the next instruction to be fetched	1
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	
the address contained in the PC (program counter) is copied to the MAR (memory address register) via the address bus	
the address part of the instruction, if any, is placed in the MAR (memory address register)	
the value in the PC (program counter) is then incremented so that it points to the next instruction to be fetched	

Examiner's Comments on Question 7 (a) and (b)

Part (a) was answered very well with most candidates able to gain two marks.
In part (b) very few candidates gained full marks despite the range of responses they could have given. Most candidates demonstrated a need to improve their knowledge of the fetch-execute cycle. Many candidates gained just one mark for the incrementation of the program counter. Some candidates gained three marks for identifying some correct stages.

Q 2) Winter 2015 P13

3 A section of computer memory is shown below:

Address	Content
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
1000 1100	
1000 1101	
1000 1110	
1000 1111	

(a) (i) The contents of memory location 1000 0001 are to be read.
Show the contents of the Memory Address Register (MAR) and the Memory Data Register (MDR) during this read operation: [2]

MAR | | | | | | | | |

MDR | | | | | | | | |

(ii) The value 0111 1001 is to be written into memory location 1000 1110.
Show the contents of the MAR and MDR during this write operation: [2]

MAR | | | | | | | | |

MDR | | | | | | | | |

(iii) Show any changes to the computer memory following the read and write operations in **part (a)(i)** and **part (a)(ii)**. [1]

Address	Content
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
1000 1100	
1000 1101	
1000 1110	
1000 1111	

(b) Name **three** other registers used in computers.

1 .....

2 .....

3 ..... [3]

(c) The control unit is part of a computer system.

What is the function of the control unit?.....

.....

.....

.....

..... [3]

Examiners' Comments Question 3 (a), (b) and (c)

In part (a) some candidates were able to recognise and select the correct address and contents. Candidate need to make sure they read the whole question before answering as some had not noted the correct memory location provided in the question. Some candidates were able to provide the correct contents of the second set of registers, but some candidates did not manage to recognise how a section of memory worked and could not provide a correct answer to the question.

In part (b) some candidates could provide three correct registers, but many could only provide one or two.

In part (c) many candidates demonstrated limited knowledge of the workings of the control unit. Most were vague in their description and needed specific detail about how the unit operates.

Q 3) Winter 2016 P12

6 Four computer terms and **eight** descriptions are shown below.
Draw lines to connect each computer term to the correct description(s). [4]

Computer term	Description
Arithmetic and logic unit (ALU)	Data can be read but not altered
	Carries out operations such as addition and multiplication
Control unit	
	Stores bootstrap loader and BIOS
	Fetches each instruction in turn
Random access memory (RAM)	
	OR, NOT
	Stores part of the operating system currently in use
Read only memory (ROM)	Stores data currently in use
	Manages execution of each instruction

Examiner Report
The full range of marks was seen from candidates in this question on terms and descriptions. Some candidates only connected a single line from each computer term. The question stated to draw lines, candidates should note this type of question means that there may be more than one line that can be drawn to connect terms to description. If a question states to draw a line, this is when only a single line should be drawn from each term to a description.

Q 4) Winter 2016 P11& 13

1 To process an instruction, a central processing unit (CPU) goes through a cycle that has three main stages.
Name each stage in this cycle.
Stage 1 .....
Stage 2 .....
Stage 3 ..... [3]

Examiner Report Question 1
Some candidates could correctly identify the three stages of processing an instruction, some managed to identify fetch and execute, but not decode. Some could not identify any correct stages. The most common incorrect answer given by candidates was input, process, output. This was not a specific enough answer for candidates to gain the marks.

Q 5) Summer 2017 P12

1 Name **three** different buses that are used in the fetch-execute cycle.

Bus 1 .....

Bus 2 .....

Bus 3 ..... [3]

Examiner Comment on Q 1

Many candidates provided three correct busses. The most common incorrect answer was candidatesproviding fetch, decode and execute, which demonstrated a misunderstanding of the question.

Q 6) Winter 2017 P13

4 Six components of a computer system and six descriptions are shown.

Draw a line to match each component with the most suitable description. [5]

Component	Description
Arithmetic Logic Unit (ALU)	Used to connect together the internal components of the CPU.
Buses	Used to carry out calculations on data.
Control Unit(CU)	Used to temporarily hold data and instructions during processing.
Immediate Access Store (IAS)	Used to allow interaction with the computer.
Input/ Output	Used to hold data and instructions before they are processed.
Registers	Used to manage the flow of data through the CPU.

Q 7) March 2018 P12 (India)

10 The table shows a segment of primary memory from a Von Neumann model computer.

Address	Contents
10001	11001101
10010	11110001
10011	10101111
10100	10000110
10101	00011001
10110	10101100

The program counter contains the data 10010.

(a) (i) State the data that will be placed in the memory address register (MAR).

.....[1]

(ii) State the data that will be placed in the memory data register (MDR).

.....[1]

(b) Describe the stored program concept when applied to the Von Neumann model.

.....

.....

.....

.....

.....

.....

.....

.....[4]

Comments on Question 10

(a) (i) and (ii) *Most candidates provided a correct response and demonstrated an excellent level o f understanding.*

(b) *This question appeared to be very challenging for candidates. Many candidates described the f etch execute cycle. It would be helpful if candidates understood that the stored program concept is a specific infrastructure for the central processing unit and not the fetch execute cycle. It would be encouraging to see candidates demonstrate a more confident level of knowledge of the stored pro gram concept.*

Q 8) Summer 2018 P11

5 Six components of the Von Neumann model for a computer system and **six** descriptions are given. Draw a line to match each component to the most suitable description. [5]

Component	Description
Immediate access store(IAS)	Holds data and instructions when they are loaded from main memory and are waiting to be processed.
Register	Holds data temporarily that is currently being used in a calculation.
Control unit(CU)	Holds data or instructions temporarily when they are being processed.
Accumulator(ACC)	Manages the flow of data and interaction between the components of the processor.
Arithmetic logic unit (ALU)	Carries out the calculations on data.
Bus	Pathway for transmitting data and instructions.

Q 9) Summer 2018 P12

6 Kelvin correctly answers an examination question about the Von Neumann model.

Eight different terms have been removed from his answer.

Complete the sentences in Kelvin's answer, using the list given. Not all items in the list need to be used.

• accumulator (ACC) • address bus • arithmetic logic unit (ALU)
• control unit (CU) • data bus • executed
• fetches • immediate access store (IAS)
• memory address register (MAR) • saved
• memory data register (MDR) • program counter (PC) • transmits

The central processing unit (CPU) .....the data and instructions needed and stores them in the..... to wait to be processed. The ..... holds the address of the next instruction. This address is sent to the ..... The data from this address is sent to the ..... .

The instruction can then be decoded and ..... .

Any calculations that are carried out on the data are done by the..... . During calculations, the data is temporarily held in a register called the .....[8]

Q 10) Winter 2018 P13

11 The fetch-execute cycle make use of registers.

(a) Describe the role of the Program Counter (PC).

.....

.....

.....

..... [2]

(b) Describe the role of the Memory Data Register (MDR).

.....

.....

.....

..... [2]

Q 11) Summer 2019 P12

3 Vanessa writes a paragraph as an answer to an examination question about the central processing unit (CPU).

Use the list given to complete Vanessa's answer by inserting the correct **six** missing terms.

Not all terms will be used.

• Components	• Data	• Decoded
• Executed	• Fetched	• Instructions
• RAM	• ROM	• Secondary storage

The CPU processes ..... and ..... .

An instruction is ..... from ..... into the CPU where it is then ..... . Once this has taken place the instruction is then ..... . [6]

Q 12) Winter 2019 P13

7 The Von Neumann model for a computer system has several components that are used in the fe tch-execute cycle.

(a) One component is main memory.

(i) Describe what is meant by main memory and how it is used in the Von Neumann model for a co mputer system.

.....

.....

.....

.....

..... [3]

(ii) State **two** other components in the Von Neumann model for a computer system.

1 .....

2 ..... [2]

(b) Computer systems often use interrupts.

Five statements are given about interrupts.

Tick (✓) to show if each statement is **True** or **False**. [5]

Statement	**True (✓)**	**False (✓)**
Interrupts can be hardware based or software based		
Interrupts are handled by the operating system		
Interrupts allow a computer to multitask		
Interrupts work out which program to give priority to		
Interrupts are vital to a computer and it cannot function without them		

Q 13) Winter 2019 P12

2 The Von Neumann model for a computer system uses several components in the fetch-execute cycle. One component that is used is the Control Unit (CU).

Identify **four** other components that are used in the Von Neumann model for a computer system.

1 .....

2 .....

3 .....

4 ..... [4]

Q 14) March 20 P12

1 The Von Neumann model for a computer system uses components, such as registers and buses, in the fetch-execute cycle.

(a) Draw a line to connect each component to its correct description. [3]

Component	Description
Control Bus	Increments to point to the address of the next instruction to be fetched
Program Counter (PC)	Holds the result of a calculation. It is located within the Arithmetic Logic Unit (ALU)
Memory Data Register (MDR)	Carries signals to synchronise the fetch-execute cycle
Accumulator (ACC)	Temporary storage between the Central Processing Unit (CPU) and primary memory

(b) State **two** buses, other than the control bus, used in the Von Neumann model for a computer system.

1 .....

2 ..... [2]

Q 15) Summer 20 P12

1 A Von Neumann model for a computer system has a central processing unit (CPU) that makes use of registers.

(a) Identify **three** registers that may be used.

Register 1 .....

Register 2 .....

Register 3 ..... [3]

(b) The CPU is responsible for processing instructions.

One stage of processing instructions is the decode stage.

(i) Identify the **two other** stages of processing instructions.

Stage 1 .....

Stage 2 ..... [2]

(ii) Identify the component of the CPU that is responsible for decoding instructions.

..... [1]

Q 16) 15a Summer 20 P11

5 Six components of a computer are given.
Some are part of the central processing unit (CPU) of the Von Neumann model for a computer system.
Tick (✓) to show if each component is a **CPU component** or is **Not a CPU component**. [6]

Component	**CPU component (✓)**	**Not a CPU component (✓)**
Arithmetic logic unit (ALU)		
Hard disk drive (HDD)		
Memory address register (MAR)		
Random access memory (RAM)		
Solid state drive (SSD)		
Control unit (CU)		

Q 17) Winter 20 P13

2 Paige has a computer that has a central processing unit (CPU) based on the Von Neumann model for a computer system.
(a) Identify the component within the CPU that controls the flow of data.
..... [1]
(b) Identify the component within the CPU where calculations are carried out.
..... [1]
(c) Identify the component within the CPU that stores the address of the next instruction to be processed.
..... [1]
(d) Identify the register within the CPU that holds an instruction that has been fetched from memory.
..... [1]
(e) Identify the register within the CPU that holds data that has been fetched from memory.
..... [1]

Q 18) March 20 P12

8 The Von Neumann model, for a computer system, uses the stored program concept.
(a) Describe what is meant by the stored program concept.
.....
.....
.....
..... [2]

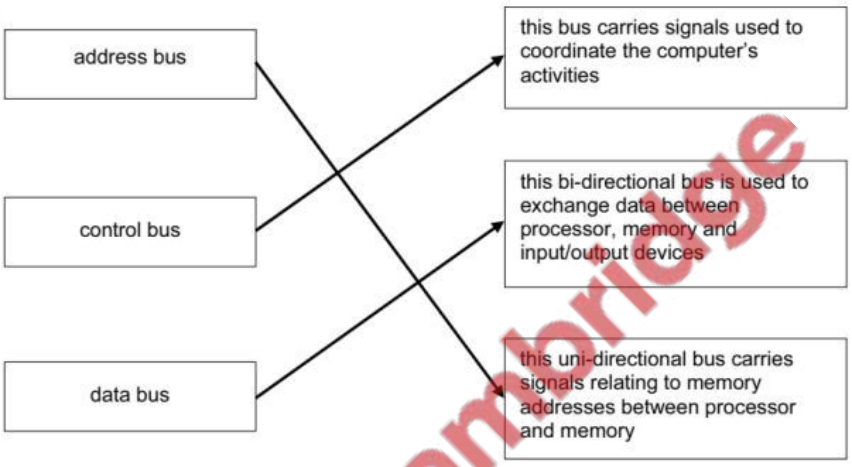
(b) The fetch-execute cycle of a Von Neumann model, for a computer system, uses registers and buses.
(i) Describe the role of the Program Counter.
.....
.....
.....
..... [2]
(ii) Describe the role of the Control Bus.
.....
.....
.....
..... [2]

(c) Computers based on the Von Neumann model, for a computer system, use interrupts. Explain why interrupts are needed.

……
……
……
…… [2]

Marking Scheme

7 (a)



(b)

description of stage	sequence number
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register)	3
the instruction is finally decoded and is then executed	7
the PC (program counter) contains the address of the next instruction to be fetched	*(1)*
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	4
the address contained in the PC (program counter) is copied to the MAR (memory address register) via the address bus	2
the address part of the instruction is placed in the MAR (memory address register)	6
the value in the PC (program counter) is then incremented so that it points to the next instruction to be fetched	5*

The incrementation of the program counter can appear at any stage after 2. All other stages must be in the correct given order. [6]

Q 2) Winter 2015 P13

3 (a) (i)

MAR	1	0	0	0	0	0	0	1

MDR	0	1	0	1	0	0	0	1

(ii)

MAR	1	0	0	0	1	1	1	0

MDR	0	1	1	1	1	0	0	1

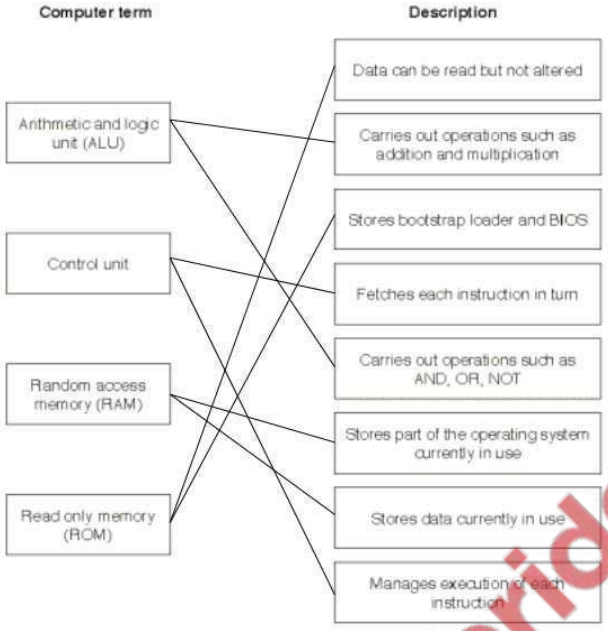
(iii)

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
1000 1100	
1000 1101	
1000 1110	**0111 1001**
1000 1111	

(b) – CIR (Current Instruction Register)
– PC (Program Counter)
– Acc (Accumulator)

(c) – Controls operation of memory, processor and input/output
– Instructions are interpreted
– Sends signals to other components telling them "what to do"

Q 3) Winter 2016 P12



[4]

Q 5) Summer 2017 P12

Question	Answer	Marks
1	∞ address (bus) ∞ control (bus) ∞ data (bus)	3

Q 6) Winter 2017 P13

Question	Answer	Marks
4	1 mark for each correct line up to a total of 5 marks Component / Description Arithmetic Logic Unit (ALU) → Used to carry out calculations on data. Buses → Used to connect together the internal components of the CPU. Control Unit (CU) → Used to manage the flow of data through the CPU. Immediate Access Store (IAS) → Used to temporarily hold data and instructions during processing. Input/Output → Used to allow interaction with the computer. Registers → Used to hold data and instructions before they are processed.	5

Q 7) March 2018 P12 (India)

Question	Answer	Marks
10(a)(i)	10010	1
10(a)(ii)	11110001	1
10(b)	Any **four** from: The program is stored on a secondary storage device Data and instructions are moved to memory / RAM Data and instructions are stored in the same memory / RAM Data and instructions are moved to registers to be executed Instructions are fetched one at a time	4

Q 8) Summer 2018 P11

Question	Answer	Marks
5	1 mark for each correct line, up to a maximum of 5 marks: **Component** → **Description** Immediate access store (IAS) → Holds data and instructions when they are loaded from main memory and are waiting to be processed. Register → Holds data temporarily that is currently being used in a calculation. Control unit (CU) → Holds data or instructions temporarily when they are being processed. Accumulator (ACC) → Manages the flow of data and interaction between the components of the processor. Arithmetic logic unit (ALU) → Carries out the calculations on data. Bus → Pathway for transmitting data and instructions.	5

Q 9) Summer 2018 P12

6	1 mark for each correct missing word, in the given order: – fetches – immediate access store // IAS – program counter // PC – memory address register // MAR – memory data register // MDR – executed – arithmetic logic unit // ALU – accumulator // ACC	8

Q 10) Winter 2018 P13

Question	Answer	Marks
11(a)	∝ Holds address of next/current instruction … ∞ … to be fetched/processed/executed	2
11(b)	∝ Stores data/instruction **that is in use …** ∞ … from address in MAR	2

Q 11) Summer 2019 P12

3	1 mark for each correct term, in the correct place: – Data/instructions – Instructions/data (must be the alternative to MP1) – Fetched – RAM – Decoded – Executed	**6**

Q 12) Winter 2019 P13

Question	Answer	Marks
7(a)(i)	**Three** from: ∞ RAM ∞ Primary memory ∞ Volatile memory ∞ Holds currently in use data/instructions ∞ Directly accessed by the CPU	**3**
7(a)(ii)	**Two** from: ∞ Arithmetic and logic unit (ALU) ∞ Memory address register (MAR) ∞ Memory data register (MDR) // Memory buffer register (MBR) ∞ Accumulator (ACC) ∞ Immediate Access Store (IAS) ∞ Control Unit (CU) ∞ Program counter (PC) ∞ Current instruction register (CIR) ∞ Address bus ∞ Data bus ∞ Control bus ∞ Input device ∞ Output device ∞ Secondary storage device	**2**

Question	Answer	Marks
7(b)	**One** mark for each correct row	**5**

Statement	True (✔)	False (✔)
Interrupts can be hardware based or software based	✓	
Interrupts are handled by the operating system	✓	
Interrupts allow a computer to multitask	✓	
Interrupts work out which program to give priority to		✓
Interrupts are vital to a computer and it cannot function without them	✓	

Q 13) Winter 2019 P12

2210/12 | Cambridge O Level – Mark Scheme PUBLISHED | October/November 2019

Question	Answer	Marks
2	**Four** from: ∞ Arithmetic and logic unit (ALU) ∞ Memory address register (MAR) ∞ Memory data register (MDR) // Memory buffer register (MBR) ∞ Accumulator (ACC) ∞ Immediate Access Store (IAS) ∞ Main memory // RAM ∞ Program counter (PC) ∞ Current instruction register (CIR) ∞ Address bus ∞ Data bus ∞ Control bus ∞ Input device ∞ Output device ∞ Secondary storage device	4

Q 14) March 20 P12

0478/12 | Cambridge IGCSE – Mark Scheme PUBLISHED | March 2020

Question	Answer	Mark
1(a)	**Component** / **Description** Control Bus → Carries signals to synchronise the fetch-execute cycle Program Counter (PC) → Increments to point to the address of the next instruction to be fetched Memory Data Register (MDR) → Temporary storage between the Central Processing (CPU) and primary memory Accumulator (ACC) → Holds the result of a calculation. It is located within the Arithmetic Logic Unit (ALU) 1 mark for 1 correct line 2 marks for 2 correct lines 3 marks for 3/4 correct lines	3
1(b)	Any **two** from: • Address bus • Data bus	2

Q 15) Summer 20 P12

2210/12 | Cambridge O Level – Mark Scheme PUBLISHED | May/June 2020

Question	Answer	Marks
1(a)	Any **three** from: – MAR – MDR // MBR – PC // IAR // NIR // SCR – ACC – CIR // IR – IAS	3
1(b)(i)	– Fetch – Execute	2
1(b)(ii)	– Control unit	1

Q 16) 15a Summer 20 P11

5		6

Component	CPU component (✓)	Not a CPU component (✓)
Arithmetic logic unit (ALU)	✓	
Hard disk drive (HDD)		✓
Memory address register (MAR)	✓	
Random access memory (RAM)		✓
Solid state drive (SSD)		✓
Control unit (CU)	✓	

One mark per each correct row

Q 17) Winter 20 P13

2(a)	– Control unit // CU	1
2(b)	– Arithmetic logic unit // ALU	1
2(c)	– Program counter // memory address register // PC // MAR	1
2(d)	– Memory data register // current instruction register // MDR // CIR	1
2(e)	– Memory data register // MDR	1

Q 18) March 20 P12

8(a)	– **Instructions** and **data** stored in the same/main memory – Instructions fetched and executed in order / one after another / in sequence	2
8(b)(i)	– Holds the **address** … – … of **next** / **current** instruction	2
8(b)(ii)	Any **two** from: – Carries / transfers **control** signals/instructions // carries/transfers commands … – … from CPU/CU to components // from devices to CPU/CU – To synchronise the FE cycle	2
8(c)	Any **two** from: – To identify that the processor's attention is required // to stop the current **process/task** – To allow multitasking – To allow for efficient processing // prioritising actions – To allow for efficient use of hardware – To allow time-sensitive requests to be dealt with – To avoid the need to poll devices	2