OCR
RECOGNISING ACHIEVEMENT

GCE

Electronics

Advanced GCE **2530**

Control Circuits

Mark Scheme for June 2010

Oxford Cambridge and RSA Examinations

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Question			Expected Answer	Mark	Rationale
1	(a)		General Purpose Register Holds bytes/words transferred from the accumulator Can hold values, temporary storage, etc	 **[1]** **[1]**	
	(b)		Fetch-execute Cycle Sequence of CPU operations, repeated continually Identification of sequence Any two relevant points accepted	 **[1]** **[1]**	
	(c)		Subroutine A separate section of a program that performs a specific function Any two from: • Used repeatedly • Saves on programme time • Reduces memory space • Can be used in other programmes • Called from within the main program	 **[1]** **[1]**	
	(d)		Handshaking Two-way exchange of information To synchronise	 **[1]** **[1]**	Allow reference to flip-flops and input / output

<table>
<tr><th colspan="3">Question</th><th>Expected Answer</th><th>Mark</th><th>Rationale</th></tr>
<tr><td colspan="3"></td><td></td><td></td><td></td></tr>
<tr><td>2</td><td>(a)</td><td>(i)</td><td>Correct circuit symbol for a tristate
Appropriate labels for input, output and enable
Allow if Enable drawn as "active low"</td><td>[1]
[1]</td><td></td></tr>
<tr><td colspan="3"></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>(ii)</td><td><table><tr><th>Enable</th><th>Input</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>-</td></tr><tr><td>0</td><td>1</td><td>-</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>Correct Input/Enable in any order
(Accept "active low" truth table)
Correct Output
("Undetermined" conditions must be clear for the mark to be awarded)</td><td>

[1]

[1]</td><td>Allow “float” for “undetermined”</td></tr>
<tr><td colspan="3"></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>(iii)</td><td>Only 1 device "connected" at any one time
Used to isolate stored data in memory</td><td>[1]
[1]</td><td>Allow reference to multiple devices</td></tr>
<tr><td colspan="3"></td><td></td><td></td><td></td></tr>
<tr><td>3</td><td>(a)</td><td>(i)</td><td>A – Gate</td><td>[1]</td><td></td></tr>
<tr><td colspan="3"></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Triac is made to conduct by sinking or sourcing current through gate
When conducting, triac can only be turned off by cutting current mt1/mt2
When AC passes through zero then triac stops conducting</td><td>[1]
[1]
[1]</td><td></td></tr>
<tr><td colspan="3"></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>(iii)</td><td>AC – current passes through zero every half cycle (mains – 10ms)
DC – has to be switched off to set current to zero</td><td>[1]
[1]</td><td></td></tr>
<tr><td colspan="3"></td><td></td><td></td><td></td></tr>
</table>

Question			Expected Answer	Mark	Rationale
	(b)	**(i)**	Use of potential divider rule Voltage at A =(50/(50+100))* 6 =2V	**[1]** **[1]** **[1]**	Allow any valid rule with correct values
		(ii)	Voltage of power supply = 2.5 * ((100+50)/50) = 7.5 V	**[1]** **[1]**	Allow any valid rule with correct values
		(iii)	Triac has very low resistance when conducting and much lower than that of motor High current passes through triac Fuse blows so shutting off triac as current goes to zero	**[1]** **[1]** **[1]**	
4	**(a)**	**(i)**	A – Thermistor	**[1]**	
		(ii)	As the temperature increases, the resistance of the thermistor falls Resistance of R remains the same so greater proportion of 15V supply falls across R $V_{(temp)}$ increases and potential at Xrises nearer to 15V	**[1]** **[1]** **[1]**	
		(iii)	V(ref) increases and op amp saturates positively so heater turns on, raising temperature of animal house Thermistor detects higher temperature and its resistance decreases Voltage at V- increases towards V(ref) value V- reaches V+ value thermistor still responding so V- goes beyond V(ref), begins to cool and V- begins to oscillate around V(ref) value	**[1]** **[1]** **[1]** **[1]** **[1]**	
		(iv)	When output of op amp attempts to saturate negatively, the voltage at point Q is held at -0.7V When the voltage at point Q drops below zero, the diode D becomes forward biased and in forward biased mode the diode maintains a voltage of -0.7V across itself and holds Q at -0.7V	**[1]** **[1]**	

Question			Expected Answer	Mark	Rationale
	(b)	**(i)**	Correct symbol for op amp with V+ connected to zero volts Correct position for resistor Correct position for capacitor	**[1]** **[1]** **[1]**	
		(ii)	Any of the following for 1 mark, up to a maximum of 4 marks: • avoids hunting/overload/oscillation of final temperature • output of ramp generator rises/falls with time depending on input from difference amplifier • as W and X get closer, output of difference amplifier gets smaller • rate of change of ramp generator output decreases with decreasing input • heater power increases gradually at an ever slower rate until W = X	**[4]**	
5	**(a)**	**(i)**	Clock – an oscillator that feeds regular pulses into the CPU	**[1]**	Allow “control operations”
		(ii)	Address Bus – carries information containing the location of data from CPU to memory	**[1]**	
		(iii)	Data Bus – carries data to and from CPU and memory	**[1]**	Allow reference to input / output
	(b)	**(i)**	Correct answer – AF	**[1]**	
		(ii)	Correct answer – 1101 0100	**[1]**	
	(c)		Inputs and outputs correctly labelled D and Q correctly linked with inputs and outputs respectively Enable connected to clock of each D-type	**[1]** **[1]** **[1]**	

Question			Expected Answer	Mark	Rationale
6	(a)	(i)	Correct arrangement of inputs Correct arrangement of outputs	[1] [1]	
		(ii)	The value of RD would be set high when required (or wtte)	[1]	With reference to (a) (i) arrangement
	(b)	(i)	D-type flip-flop Accept flip-flop	[1]	
		(ii)	IO line is used to write information into cell as well as read from it (or wtte)	[1]	
	(c)	(i)	Write to cell – RD held low to tristate enable so insolating flip-flop outputs Q from bus Word on data bus is stored when WR goes high and clocks flip-flops	 [1] [1]	
		(ii)	Read from cell – WR held low so flip-flop is not clocked RD goes high to enable of tristate to connect flip-flops to data bus	 [1] [1]	
7	(a)		A1 F7 = *reset D-type + letter A* A2 CE = *reset D-type + letter C* A3 CF = *reset D-type + letter E* A4 **B7** = *reset D-type + letter H* A5 **8E** = *reset D-type + letter L* A6 **E7** = *reset D-type + letter P* A7 **DB** = *reset D-type + letter S*	 [1] [1] [1] [1]	

Question			Expected Answer			Mark	Rationale
	(b)		**Address**	**Contents**	**Explanation**		
			00	3E 00	move 00 into the accumulator	**[1]**	
			02	32 FF	output 00	**[1]**	
			04	32 DD	reset address DD contents to 00	**[1]**	
			06	3A EF	swallow input	**[1]**	
			08	E6 07	test if KEYPAD has been pressed	**[1]**	
			0A	C2 14	if yes then go to 14 to find out which letter it was and store it	**[1]**	
			0C	C3 06	if not return to read the input again	**[1]**	
			Correct numbering of addresses Note: Explanation not required for mark				

Question			Expected Answer			Mark	Rationale
	(c)		**Address**	**Contents**	**Explanation**		Explanation required not statement of contents
			14	C6 A0	add keypad code to A0		
			16	6F	make X = LUT address	**[1]**	
			17	7E	move letter code into Accumulator		
			18	32 EE	store letter code in temporary store	**[1]**	
			1A	3A DD	swallow number of times keypad is pressed		
			1C	C6 B0	add B0 to create address where letter code is to be stored		
			1E	6F	make X = next address in letter store	**[1]**	
			1F	3A EE	move letter code back into accumulator		
			21	77	store letter code in memory sequence	**[1]**	
			22	3A DD	reload number of key presses (or letters)		
			24	C6 01	add 1 to this number		
			26	32 DD	and restore in address DD	**[1]**	
			28	3A EF	swallow input and wait		
			2A	E6 07	until keypad button		
			2C	C2 28	has been released	**[1]**	
			2E	C3 06	return to retest for next keypad push or write button push (do not accept go to address 06 or to start)	**[1]**	
			Summary				
			Recover letter code from LUT and store at address EE			**[1]**	
			Create address where letter code is to be stored and store it in memory sequence starting from address BO			**[1]**	
			Wait until keypad button is released and then return to test for keypad or write button being pressed			**[1]**	

Question			Expected Answer			Mark	Rationale
	(d)		**Address**	**Contents**	**Explanation**		
			46	3E FF	put FF in to accumulator	**[1]**	Allow count up answer
			48	D6 01	decrement accumulator by 01	**[1]**	Allow delay of any length
			4A	C2 48	if accumulator non-zero go to 48	**[1]**	
			Correct address and code required for each line for 1 mark Note: Explanation is not required				
					QWC	**[3]**	

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